

DESIGN METHODOLOGY FOR CURRENT CONVEYOR BASED CONTINUOUS-TIME FIELD- PROGRAMMABLE ANALOG ARRAY

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ABSTRACT

A design methodology for continuous time Field-Programmable Analog Array (FPAA) is presented. After introducing the key features of FPAA and dealing with design issues related to continuous-time applications, we present the elementary cell of the proposed FPAA. This cell is based on current conveyors and designed for high-frequency applications. Two examples are presented : a high-frequency amplifier and a high-frequency multiplier.

1.1. INTRODUCTION

One defines a Field-Programmable Analog Array (FPAA) as an integrated circuit which allows, by the mean of flexible programmability facilities, to implement analog functions. If we consider the recent market increase of programmable devices such as PALs, EPLDs, FPGAs for the digital counterpart, it is obvious to say that, for real-time signal processing applications, FPAA design should provide electronics designers with a very efficient and powerful tool.

A FPPAA consists of programmable analogue elementary cells which can be interconnected by the mean of programmable interconnexions. The reconfigurable cell has to perform a set of functions, in order to provide the flexibility, with good electrical performance.

The set of functions is classically defined as : amplifier, comparator, multiplier, voltage-controlled oscillator.

The different previous approaches are operational-amplifier based and operate at limited bandwidth (100khz) and have limited linearity due to the use of MOSFET based switches. The proposed approach tries to cope with these two major hints, by the use of a current conveyor based elementary cell for the reconfigurable analogue block, allowing high-frequency continuous-time applications, and being programmable as a pass or no-pass switch by tuning its bias sources.

1.2. DESIGN ISSUES FOR FIELD-PROGRAMMABLE ANALOG ARRAY

Design of analog applications requires attention to several parameters like noise level, distortion, dynamic range, etc. The two major key features for the design of an efficient and useful analog array are the programming of the elementary functions and the reconfigurable topology. The elementary cell function is set by changing some parameters like the value of programmable transconductances and capacitors. The programmed cell has to perform its function with good electrical performance offering wide parameter range for a flexible analog array. Two different approaches, the continuous-time or the switched approach, can be considered. These two techniques do not offer the same trade-offs between performance and parameter range for the programming.

The switched approach consists of switched-capacitors or switched-current which are digitally controlled and provide a wide parameter range but with frequencies limited to few hundred kilohertz because of the Shannon theorem [1-2-3].

The continuous-time approach offer a lower parameter range compared to the switched approach, but with particular design techniques, like the use of current conveyor for example, some very efficient analog blocks can be developed for the analog array. In the previous works [4-5] using the continuous-time approach for the design of field-programmable analog array, the performance of the circuit were limited by the use of both Op-Amp based design and analog switches, preventing high-frequency operation of the circuits.

A new methodology for the elementary analog cell design is introduced, and a specific approach for the interconnection of the cells without the use of switches in the signal path is addressed. Several properties of current conveyors are used to achieve both a high-frequency operation of the elementary cells and a local interconnection scheme. The configuration of the circuit, the programming of the functions and of the topology

require the used of bit registers and control voltages. Some registers are converted with a digital to analog converter to provide control voltages to set the value of the programmable transconductances and capacitors of the array [6]-[7]. The control voltages are locally stored, near the element to program, on a capacitor which needs to be periodically refreshed. New configuration techniques have been recently addressed, as for example the use of EEPROM non-volatile analog memory. This technique has been thoroughly studied in [8]. The present paper focuses on the design of the analog cell, and the configuration of the analog array and its architecture are not addressed.

1.3. ELEMENTARY ANALOG CELL

The analog elementary cell of the array, presented in figure 1, consists of a four MOSFET transconductor and two conveyor-based I-V converters. The four MOSFET transconductor [9-10] is a highly linear differential, programmable transconductor with response given by:

$$(I_{xp} - I_{xn}) = \mu C_{ox} \frac{W}{L} (V_{c1} - V_{c2})(V_{Ep} - V_{En}) \quad (1)$$

Parameters μ and C_{ox} are respectively the average carrier mobility in the channel and the gate oxide capacitance per unit area. L and W are respectively the length and the width of the transistor. Relation (1) is true if the conditions $V_{c1}, V_{c2} < \min[V_{c1} - V_T, V_{c2} - V_T]$ are verified. (V_T is the threshold voltage for a MOS transistor)

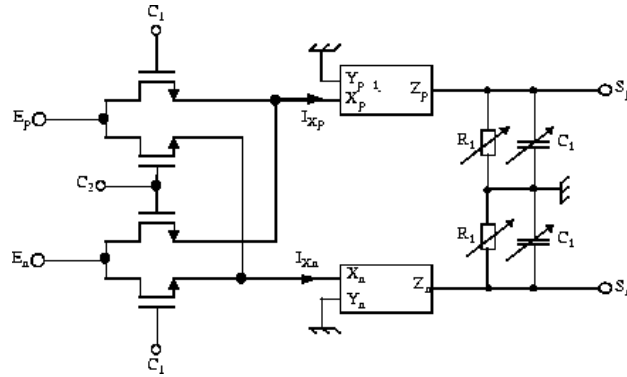


Figure 1:Elementary Analog Cell.

A current conveyor (CC) [11] is a three terminal device which operates such that if a voltage is applied to the input terminal Y, an equal potential will appear on the input terminal X. In a similar fashion, an input current forced into terminal X will result in an equal current flowing into terminal Z.

The two CCs of figure 1 perform the I-V conversion. Virtual grounds at nodes X have to be created in order to make the four MOSFET transconductor to behave linearly. The currents I_{Xp} and I_{Xn} flowing into the X nodes produce the voltages V_{Sp} and V_{Sn} . Using equation (1) the following relation is derived:

$$\frac{V_{Sp} - V_{Sn}}{V_{Ep} - V_{En}} = \frac{R_1}{1 + sR_1C_1} \mu C_{OX} (V_{C1} - V_{C2}) \quad (2)$$

The difference ($V_{C1} - V_{C2}$) is used to perform a four-quadrant analog multiplier and to control the polarity of the output signal. The load resistor and capacitor are used to performed either an amplifier or an integrator or a low-pass first order filter.

The programmable resistor R_1 is a CMOS resistor with transistors operating in ohmic region [12], in order to have both good linearity and parameter range. The programmable capacitor is based on a capacitive multiplier thoroughly described in [13].

The design of an analog processing application is performed by cascading two CCs. The output port Z of the first CC is connected to the input port Y of the second CC. If several CCs port Z are connected to the same node, then the output currents are added and converted in voltage with a resistor before going to the next stage.

As explained in the next section, a CC is biased by two current sources, a positive and a negative one. A CC can perform interconnection between cells, simulating a pass switch or a non-pass switch by turning respectively on or off its two bias current sources [14]. The CC's equivalent input impedance is modified with the polarisation.

1.4. HIGH-FREQUENCY CONSIDERATIONS

In the presented analog elementary cell the two current conveyors are used to transfer the current from the four MOSFET transconductor to the load. The frequency limitation is due to the current transfer I_z/I_x . The schematic of a current conveyor, presented in figure 2, shows that the current transfer between terminal X and Z is performed by two current mirrors M6-M8 and M7-M9. The voltage at node Y is copied to node X using the current mirrors M1-M2 and M3-M4. The transistors M10, M11, M12 and M13 are the bias current sources controlled by two voltages V_p and V_n .

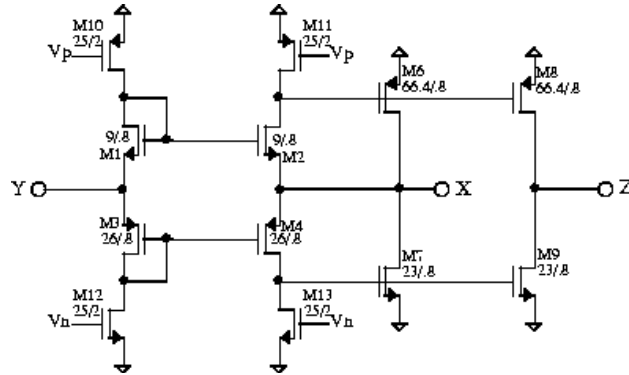


Figure 2: Schematic of the current conveyor

It can be shown that for the elementary current mirror of figure 3, the approximate first order transfer functions is:

$$I_{OUT} = gV_{OUT} = -\frac{I_{IN}gm_2}{gm_1} \frac{1 - s \frac{Cgd2}{gm_2}}{1 + s \left(\frac{C + Cgd2}{g} + \frac{Cgs1 + Cgd2}{gm_1} + \frac{gm_2 Cgd2}{gm_1 g} \right)}$$

$$\text{with } g = \frac{1}{R_L} + gds_2 \text{ and } C = Cdb_2 + C_L$$

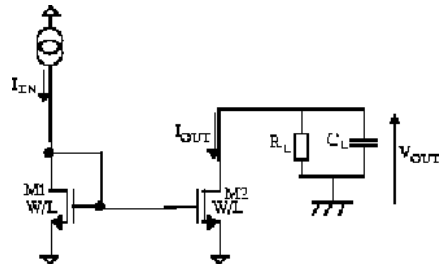
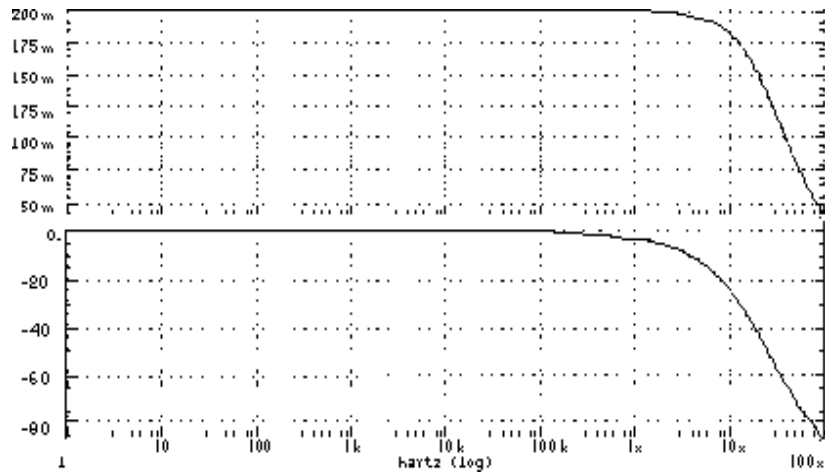


Figure 3: A simple current mirror.

$gm_{1,2}$ are the transconductance of respectively transistor M1 and M2. C_{gd2} and C_{db2} are respectively the gate-drain capacitance and drain-bulk capacitance of transistor M2. C_{gs1} is the gate-source capacitance of transistor M1.

The main limitation are due to the C_{gd2} capacitor and to the load impedance of the current mirror. If low R_1 and C_1 value are used, referring to figure 1, and reasonable W/L ratios are used to limit the C_{gd2} value, a high-frequency operation can be achieved. The current conveyor has been implemented using AMS 0.8 μ m CMOS technology previously used in [15] and chosen for its stability as far as process parameters are concerned. HSpice simulations have been carried out and a bandwidth greater than 100MHz for the current transfer is achieved using the W/L ratios given in figure 2.

1.5. RESULTS



Output voltage: magnitude (upper curve), phase (lower curve)

Figure 4: Ccs based amplifier.

The frequency response of the elementary cell (see figure 4) used as an amplifier with a 20mV input signal for a voltage gain of 10 achieves 10Mhz bandwidth (-3dB cut-off frequency).

A frequency doubler can be performed using the four MOSFET transconductor as an analog multiplier and two input signals with the same frequency. Figure 5 shows that the circuit is able to perform well as a frequency doubler at 80MHz, for two 40MHz input signals.

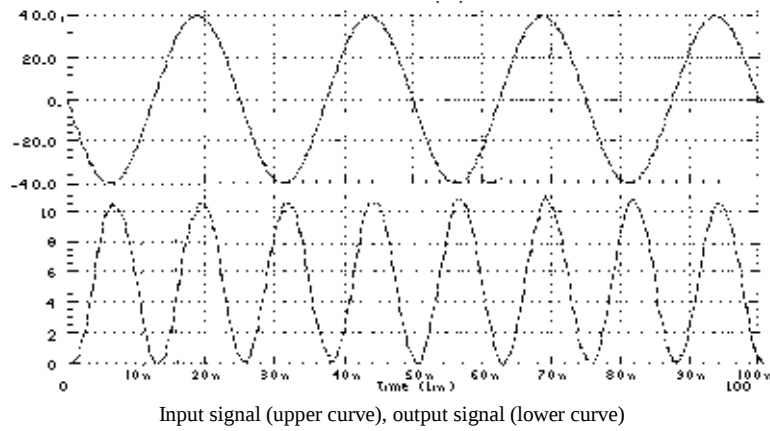


Figure 5: Ccs based frequency doubler.

1.6. CONCLUSION

A new approach for designing analog elementary cell for field-programmable analog array has been described. Its major improvement, compared to the previous works, is the use of current conveyors in order to achieve a wide range of analog functions operating at high-frequency (80 MHz). The key performance feature of the proposed approach is the current-mode processing which seems to provide attractive solution for wide bandwidth capability.

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