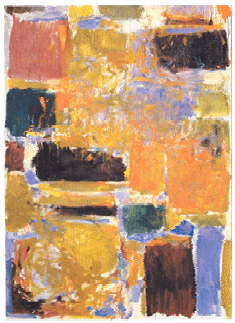

Digital Integrated Circuits
A Design Perspective

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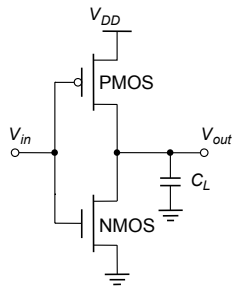
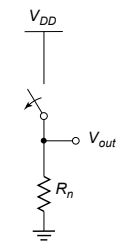
The Inverter

[Adapted from Rabaey's *Digital Integrated Circuits*, Second Edition, ©2003 J. Rabaey, A. Chandrakasan, B. Nikolic]

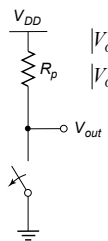
The CMOS Inverter: A First Glance



CMOS Inverter
First-order DC Analysis



$V_{in} = V_{DD}$



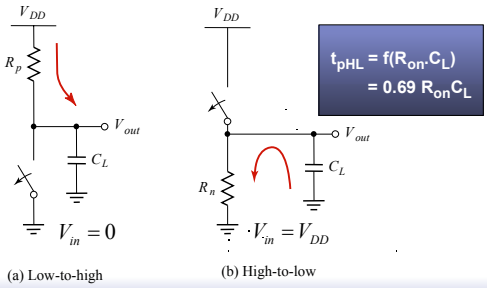
$V_{in} = 0$

$|V_{GS}| < |V_T| -> R = \infty$

$|V_{GS}| > |V_T| -> R = R_{ON}$

V_{OL} = GND
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

CMOS Inverter: Transient Response



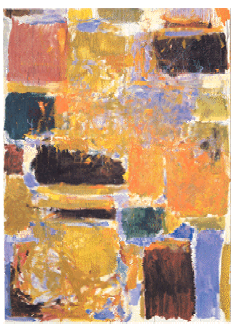
(a) Low-to-high (b) High-to-low

Inverter

CMOS Properties

- Full rail-to-rail swing ⇒ high noise margins
  - Logic levels not dependent upon the relative device sizes ⇒ transistors can be minimum size ⇒ ratioless
- Always a path to V_{dd} or GND in steady state ⇒ low output impedance (output resistance in kΩ range) ⇒ large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) ⇒ nearly zero steady-state input current
- No direct path steady-state between power and ground ⇒ no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

Inverter



Voltage Transfer Characteristic

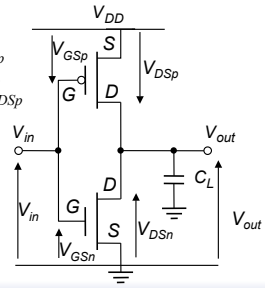
Inverter

The CMOS Inverter : Load Line

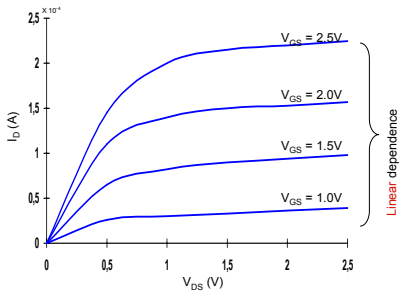
$$I_{Dn} = -I_{Dp}$$

$$V_{in} = V_{GSn}; V_{in} = V_{DD} + V_{GSp}$$

$$V_{out} = V_{DSn}; V_{out} = V_{DD} + V_{DSp}$$



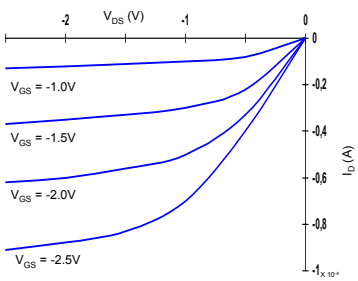
Review: Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

Review: Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed

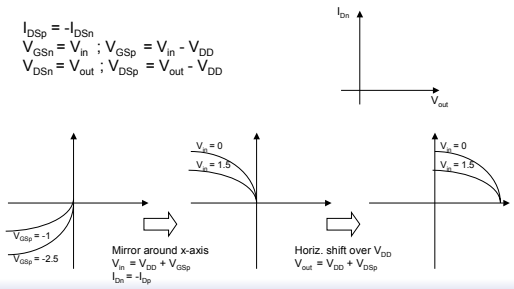


PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

Transforming PMOS I-V Lines

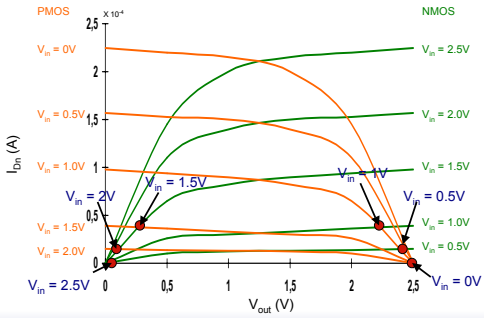
- Want common coordinate set V_{in}, V_{out}, and I_{Dn}

$I_{DSp} = -I_{DSn}$
$V_{GSn} = V_{in}$; $V_{GSp} = V_{in} - V_{DD}$
$V_{DSn} = V_{out}$; $V_{DSp} = V_{out} - V_{DD}$



Inverter

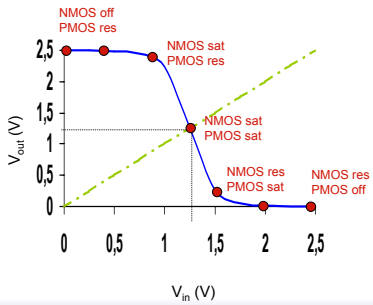
CMOS Inverter Load Lines



0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$

Inverter

CMOS Inverter VTC



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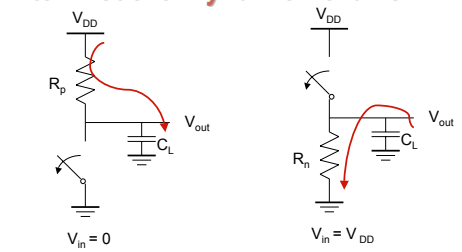
CMOS Inverter: Switch Model of Dynamic Behavior



Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

Inverter

Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

Inverter

Switching Threshold As a Function of Transistor Ratio

V_M where $V_{IN} = V_{OUT}$ (both PMOS and NMOS in saturation since $V_{GS} = V_{DS}$)

Velocity-Saturation $V_{DSAT} < V_M - V_T$

$I_{Dn} + I_{Dp} = 0$

$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tn} - \frac{V_{DSATn}}{2}\right) = 0$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}; r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

$$V_M \approx \frac{r V_{DD}}{1+r}; V_{DD} >> V_T + V_{DSAT}$$

Inverter

Switching Threshold

- V_M where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)

$$V_M \approx rV_{DD}/(1 + r) \text{ where } r = k_pV_{DSATp}/k_nV_{DSATn}$$

- Switching threshold set by the ratio r, which compares the relative driving strengths of the PMOS and NMOS transistors
- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

Switching Threshold As a Function of Transistor Ratio

$$k_nV_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_pV_{DSATp}\left(V_M - V_{DD} - V_{Tn} - \frac{V_{DSATn}}{2}\right) = 0$$

$$k = k'\frac{W}{L}$$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_nV_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k'_pV_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

Switching Threshold : Example

0.25µm CMOS

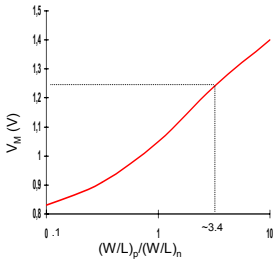
VDD=2.5V *L=0.25µm* *W=0.375µm*

	V_{T0}(V)	$\gamma(V^{0.5})$	V_{DSAT}(V)	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115.10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30.10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115\times10^{-6}}{30\times10^{-6}} \times \frac{0.63}{1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

$(W/L)_p$ = 3.5 x 1.5 = 5.25 for a V_M of 1.25V

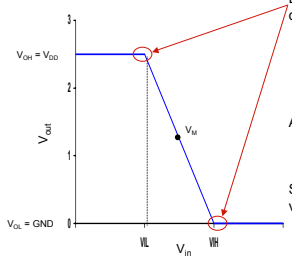
Simulated Inverter V_M



- V_M is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives V_M's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves V_M towards V_{DD}
- Increasing the width of the NMOS moves V_M toward GND

Note: x-axis is semilog

Noise Margins Determining V_{IH} and V_{IL}



A piece-wise linear approximation of VTC

By definition, V_{IH} and V_{IL} are where $dV_{out}/dV_{in} = -1$ (= gain)

$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL}$ - GND

Approximating:
$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

So high gain in the transition region is very desirable

Inverter Gain

$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right)\left(1+\lambda_n V_{out}\right)+$$

$$k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tn} - \frac{V_{DSATn}}{2}\right)\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)=0$$

$$g = \frac{dV_{out}}{dV_{in}}$$

$$g = -\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \approx \frac{1+r}{\left(V_M - V_{Tn} - V_{DSATn}/2\right)\left(\lambda_n - \lambda_p\right)}$$

Inverter Gain : Example

0.25µm CMOS

VDD=2.5V *L=0.25µm* *W=0.375µm*

	V_{T0}(V)	$\gamma(V^{0.5})$	V_{DSAT}(V)	k'(A/V^2)	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115.10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30.10^{-6}	-0.1

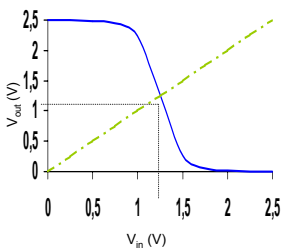
$$I_D(V_M) = 1.5\times115\times10^{-6}\times(1.25\times-0.43-0.63/2)(1+0.06\times1.25) = 59\mu A$$

$$g = \frac{1}{59\times10^{-6}}\,\frac{1.5\times115\times10^{-6}\times0.63+1.5\times3.4\times30\times10^{-6}\times1.0}{0.06+0.1} = -27.5$$

$$V_{IL} = 1.2V; V_{IH} = 1.3V; NM_L = NM_H = 1.2V$$

Inverter

CMOS Inverter VTC from Simulation



0.25um, $(W/L)_p/(W/L)_n$ = 3.4
$(W/L)_n$ = 1.5 (min size)
V_{DD} = 2.5V

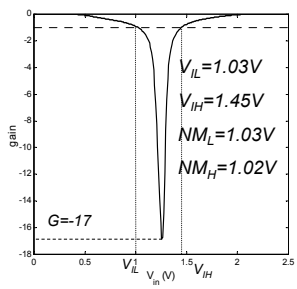
$V_M \approx 1.25V$, g = -27.5

V_{IL} = 1.2V, V_{IH} = 1.3V
$NM_L = NM_H$ = 1.2
(actual values are
V_{IL}= 1.03V, V_{IH} = 1.45V
NM_L = 1.03V & NM_H = 1.05V)

Output resistance
low-output = 2.4kΩ
high-output = 3.3kΩ

Inverter

Inverter Gain : Example Simulation



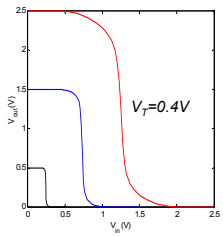
Gain is a strong function of the slopes of the currents in the saturation region, for $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

Determined by technology parameters, especially channel length modulation (λ). Only designer influence through supply voltage and V_M (transistor sizing).

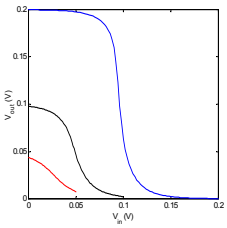
Inverter

Gain As a Function of VDD



$$g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

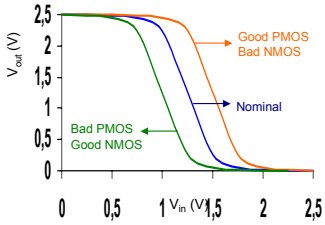
Gain As a Function of VDD



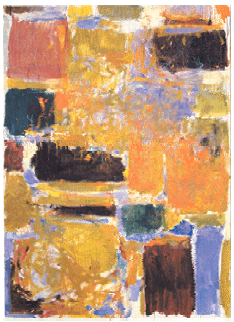
Very slow operation

EX: Watches

Impact of Process Variation on VTC Curve



Process variations (mostly) cause a shift in the switching threshold

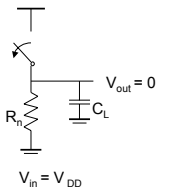


Propagation Delay

Inverter

CMOS Inverter Propagation Delay

- Propagation delay is proportional to the time-constant of the network formed by the pull-down resistor and the load capacitance



$t_{pHL} = \ln(2)\, R_{eqn}\, C_L = 0.69\, R_{eqn}\, C_L$

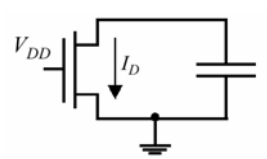
$t_{pLH} = \ln(2)\, R_{eqp}\, C_L = 0.69\, R_{eqp}\, C_L$

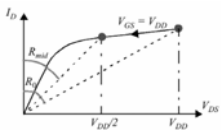
$t_p = (t_{pHL} + t_{pLH})/2 = 0.69\, C_L(R_{eqn}+R_{eqp})/2$

- To equalize rise and fall times make the on-resistance of the NMOS and PMOS approximately equal.

Inverter

Equivalent Resistance R_{EQ}





$$R_{eq} = \text{average}_{t_1 < t_2 < t_3 \ldots t_2}(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} R_{on}(t)\,dt = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}\,dt$$

$$= \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2))$$

Inverter

Equivalent Resistance R_{EQ}

Solving the integral:

$$R_{eq} = \frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2}\frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

with appropriately calculated *Idsat*

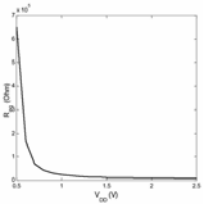
$$I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Averaging resistances:

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})}+\frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

Inverter

Equivalent Resistance R_{EQ}



W/*L*=1, *L*=0.25µ

V_{DD}(V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

Inverter

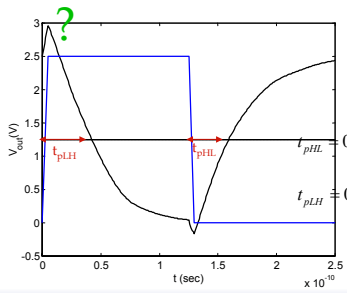
Propagation Delay

$$t_{pHL} = \ln(2)R_{eqn}C_L = 0.69R_{eqn}C_L$$
$$t_{pLH} = \ln(2)R_{eqp}C_L = 0.69R_{eqp}C_L$$

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} = 0.69C_L\left(\frac{R_{eqn}+R_{eqp}}{2}\right)$$

Inverter

Transient Response : Example



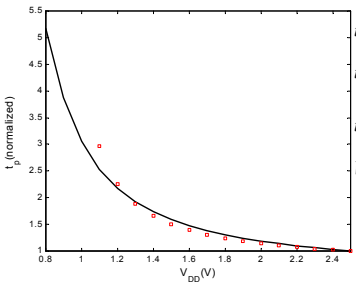
C_{LHL}=6.1fF C_{LLH}=6.0fF

$$t_{pHL} = 0.69\left(\frac{13k\Omega}{1.5}\right)\times 6.1fF = 36ps$$

$$t_{pLH} = 0.69\left(\frac{31k\Omega}{4.5}\right)\times 6.0fF = 29ps$$

Delay As a Function of V_{DD}

- To see how a designer can optimize the delay of a gate have to expand the R_{eq} in the delay equation



$$t_{pHL} = 0.69R_{eqn}C_L$$

$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}}$$

$$t_{pHL} \approx 0.52\frac{C_L}{(W/L)_n k_n' V_{DSATn}}$$

$$V_{DD} >> V_{Tn} + V_{DSATn}/2$$

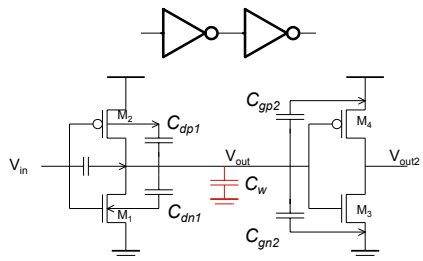
Design for Performance

- Reduce C_L
  - internal diffusion capacitance of the gate itself
    - keep the drain diffusion as small as possible
  - interconnect capacitance
  - fanout
- Increase W/L ratio of the transistor
  - the most powerful and effective performance optimization tool in the hands of the designer
  - watch out for self-loading! – when the intrinsic capacitance dominates the extrinsic load
- Increase V_{DD}
  - can trade-off energy for performance
  - increasing V_{DD} above a certain level yields only very minimal improvements
  - reliability concerns enforce a firm upper bound on V_{DD}

NMOS/PMOS Ratio

- So far have sized the PMOS and NMOS so that the R_{eq}'s match (ratio of 3 to 3.5)
  - symmetrical VTC
  - equal high-to-low and low-to-high propagation delays

NMOS/PMOS Ratio



$$C_L=(C_{dp1}+C_{dn1})+(C_{gp2}+C_{gn2})+C_W$$

NMOS/PMOS Ratio

$$\beta=\frac{(W/L)_p}{(W/L)_n}$$

$$C_L=(1+\beta)(C_{dn1}+C_{gn2})+C_W$$

$$t_p=\frac{0.69}{2}((1+\beta)(C_{dn1}+C_{gn2})+C_W)\left(R_{eqn}+\frac{R_{eqp}}{\beta}\right)$$

$$t_p=0.345((1+\beta)(C_{dn1}+C_{gn2})+C_W)R_{eqn}\left(1+\frac{r}{\beta}\right)$$

$$\beta=\beta_{opt}\rightarrow\frac{\partial t_p}{\partial\beta}=0$$

$$\beta_{opt}=\sqrt{r\left(1+\frac{C_W}{C_{dn1}+C_{gn2}}\right)}\approx\sqrt{r}$$

NMOS/PMOS Ratio

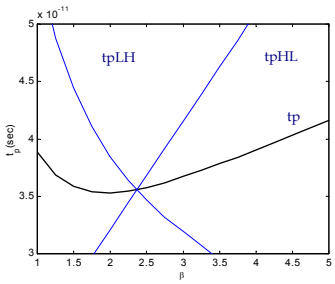
- If speed is the only concern, reduce the width of the PMOS device!
  - widening the PMOS degrades the t_{pHL} due to larger parasitic capacitance

$\beta = (W/L_p)/(W/L_n)$

$r = R_{eqp}/R_{eqn}$ (resistance ratio of identically-sized PMOS and NMOS)

$\beta_{opt} = \sqrt{r}$ when wiring capacitance is negligible

NMOS/PMOS Ratio



β of 2.4 (= 31 kΩ/13 kΩ) gives symmetrical response

β of 1.9 gives optimal performance

$\beta = W_p/W_n$

Device Sizing for Performance

- Divide capacitive load, C_L, into
  - C_{int} : intrinsic - diffusion and Miller effect
  - C_{ext} : extrinsic - wiring and fanout

$t_p = 0.69\ R_{eq}\ C_{int}\ (1 + C_{ext}/C_{int})$

$= t_{p0}\ (1 + C_{ext}/C_{int})$

- where $t_{p0} = 0.69\ R_{eq}\ C_{int}$ is the intrinsic (unloaded) delay of the gate

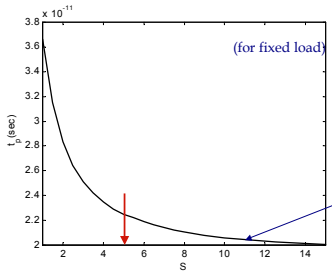
Device Sizing for Performance

- Widening both PMOS and NMOS by a factor S reduces R_{eq} by an identical factor ($R_{eq} = R_{ref}/S$), but raises the intrinsic capacitance by the same factor ($C_{int} = SC_{iref}$)

$$t_p = 0.69\, R_{ref}\, C_{iref}\, (1 + C_{ext}/(SC_{iref}))$$
$$= t_{p0}(1 + C_{ext}/(SC_{iref}))$$

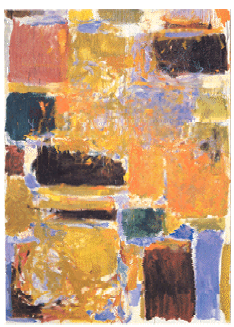
  - t_{p0} is independent of the sizing of the gate; *with no load the drive of the gate is totally offset by the increased capacitance*
  - any S sufficiently larger than (C_{ext}/C_{int}) yields the best performance gains with least area impact

Device Sizing



The majority of the improvement is already obtained for S = 5. Sizing factors larger than 10 barely yield any extra gain (and cost significantly more area).

Self-loading effect: Intrinsic capacitances dominate



Inverter Sizing

Impact of Fanout on Delay

- Extrinsic capacitance, C_{ext}, is a function of the fanout of the gate - the larger the fanout, the larger the external load.

- First determine the input loading effect of the inverter. Both C_g and C_{int} are proportional to the gate sizing, so $C_{int} = \gamma C_g$ is independent of gate sizing and

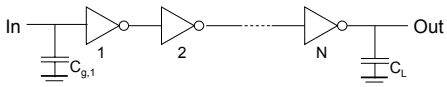
$$t_p = t_{p0}(1 + C_{ext}/\gamma C_g) = t_{p0}(1 + f/\gamma)$$

i.e., the delay of an inverter is a function of the ratio between its external load capacitance and its input gate capacitance: the effective fan-out f

$$f = C_{ext}/C_g$$

Inverter Chain

- Real goal is to minimize the delay through an inverter chain



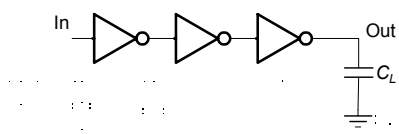
the delay of the j-th inverter stage is

$$t_{p,j} = t_{p0}(1 + C_{g,j+1}/(\gamma C_{g,j})) = t_{p0}(1 + f_j/\gamma)$$

and $t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$

so $t_p = \Sigma t_{p,j} = t_{p0} \Sigma (1 + C_{g,j+1}/(\gamma C_{g,j}))$

Inverter Chain

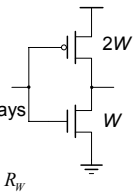


If C_L is given:
- How many stages are needed to minimize the delay?
- How to size the inverters?

May need some additional constraints.

Inverter Delay

- Minimum length devices, L=0.25μm
- Assume that for $W_P = 2W_N = 2W$
  - same pull-up and pull-down currents
  - approx. equal resistances $R_N = R_P$
  - approx. equal rise t_{pLH} and fall t_{pHL} delays
- Analyze as an RC network



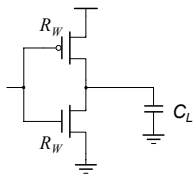
$$R_P = R_{unit}\left(\frac{W_P}{W_{unit}}\right)^{-1} \approx R_{unit}\left(\frac{W_N}{W_{unit}}\right)^{-1} = R_N = R_W$$

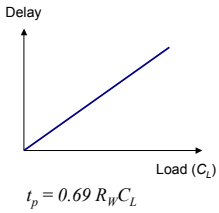
Delay (D): $t_{pHL} = (\ln 2)\, R_N C_L$ $\quad t_{pLH} = (\ln 2)\, R_P C_L$

Load for the next stage: $C_{gin} = 3 \times \frac{W}{W_{unit}} C_{unit}$

Inverter

Inverter with Load





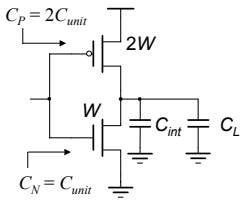
$t_p = 0.69\, R_W C_L$

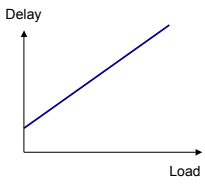
Assumptions: no load -> zero delay

$W_{unit} = 1$

Inverter

Inverter with Load





Delay = $0.69R_W(C_{int} + C_L) = 0.69R_W C_{int} + 0.69R_W C_L$
= $0.69R_W C_{int}(1 + C_L / C_{int})$
= Delay (Internal) + Delay (Load)

Inverter

Delay Formula

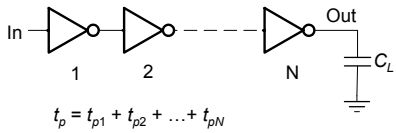
$$Delay \sim R_W (C_{int} + C_L)$$

$$t_p = 0.69 R_W C_{int} (1 + C_L / C_{int}) = t_{p0} (1 + f/\gamma)$$

$C_{int} = \gamma C_g$ with $\gamma \approx 1$
$f = C_L/C_g$ - effective fanout
$R = R_{unit}/W$; $C_{int} = WC_{unit}$
$t_{p0} = 0.69 R_{unit} C_{unit}$

Inverter

Apply to Inverter Chain



$t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$

$$t_{pj} \sim R_{unit} C_{unit} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right)$$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{i=1}^{N} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}}\right), \; C_{g,N+1} = C_L$$

Inverter

Optimal Tapering for Given N

Delay equation has N - 1 unknowns, $C_{g,2} - C_{g,N}$

Minimize the delay, find N - 1 partial derivatives $\partial t_p / \partial C_{g,j} = 0$

Result: $C_{g,j+1}/C_{g,j} = C_{g,j}/C_{g,j-1}$

Size of each stage is the geometric mean of two neighbors

$$C_{g,j} = \sqrt{C_{g,j-1} C_{g,j+1}}$$

- each stage has the same effective fanout (C_{out}/C_{in})
- each stage has the same delay

Inverter

Optimum Delay & Number of Stages

When each stage is sized by *f* and has same eff. fanout *f*:

$$f^N = F = C_L / C_{gin,1}$$

Effective fanout of each stage:

$$f = \sqrt[N]{F}$$

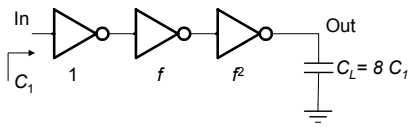
Minimum path delay

$$t_p = Nt_{p0}\left(1 + \sqrt[N]{F}/\gamma\right)$$

The relationship between t_p and F is linear for one inverter, square root for two, etc.

Inverter

Example



C_L/C_1 has to be evenly distributed across N = 3 stages:

$C_L/C_{g,1}$ = 8/1

f = $\sqrt[3]{8} = 2$

Inverter

Optimum Number of Stages N

- What is the optimal value for N given

$$f^N = F = C_L / C_{gin,1} \qquad t_p = Nt_{p0}\left(1 + \sqrt[N]{F}/\gamma\right)$$

  - if the number of stages is too large, the intrinsic delay of the stages becomes dominate
  - if the number of stages is too small, the effective fan-out of each stage becomes dominate

For a given load, C_L and given input capacitance C_{in}
Find optimal sizing *f*

$$C_L = F \cdot C_{in} = f^N C_{in} \text{ with } N = \frac{\ln F}{\ln f}$$

Inverter

Optimum Number of Stages N

$$t_p = Nt_{p0}\left(1 + F^{1/N}/\gamma\right) = \frac{t_{p0}\ln F}{\gamma}\left(\frac{f}{\ln f} + \frac{\gamma}{\ln f}\right)$$

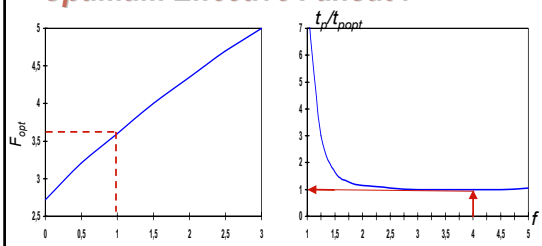
$$\frac{\partial t_p}{\partial f} = \frac{t_{p0}\ln F}{\gamma}\cdot\frac{\ln f - 1 - \gamma/f}{\ln^2 f} = 0$$

For $\gamma = 0$, $f = e$, $N = \ln F$

$$f = \exp\left(1 + \gamma/f\right)$$

Inverter

Optimum Effective Fanout f



- Choosing γ larger than optimum has little effect on delay and reduces the number of stages (and area).
  - Common practice to use f = 4 (for $\gamma = 1$)
  - But too many stages has a substantial negative impact on delay

Inverter

Normalized delay function of F

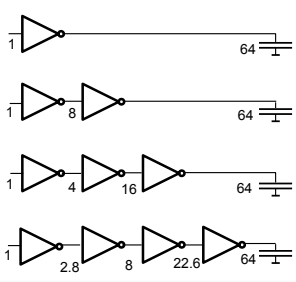
t_{opt}/t_{p0}

F ($\gamma = 1$)	Unbuffered	Two Stage Chain	Opt. Inverter Chain
10	11	8.3	8.3
100	101	22	16.5
1,000	1001	65	24.8
10,000	10,001	202	33.1

- Impressive speed-ups with optimized cascaded inverter chain for very large capacitive loads.

Inverter

Buffer Design

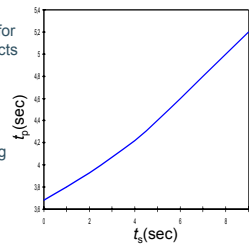


N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

Inverter

Input Signal Rise/Fall Time

- In reality, the input signal changes gradually (and both PMOS and NMOS conduct for a brief time). This affects the current available for charging/discharging C_L and impacts propagation delay.
- t_p increases linearly with increasing input slope, t_s, once $t_s > t_p$
- t_s is due to the limited driving capability of the preceding gate



Inverter

Design Challenge

- A gate is never designed in isolation: its performance is affected by both the fan-out and the driving strength of the gate(s) feeding its inputs.

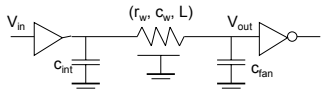
$$t^i_p = t^i_{step} + \eta\, t^{i-1}_{step} \qquad (\eta \approx 0.25)$$

- Keep signal rise times smaller than or equal to the gate propagation delays.
  - good for performance
  - good for power consumption
- Keeping rise and fall times of the signals small and of approximately equal values is one of the major challenges in high-performance designs - slope engineering.

Inverter

Delay with Long Interconnects

- When gates are farther apart, wire capacitance and resistance can no longer be ignored.



$t_p = 0.69R_{dr}C_{int} + (0.69R_{dr}+0.38R_w)C_w + 0.69(R_{dr}+R_w)C_{fan}$
where $R_{dr} = (R_{eqn} + R_{eqp})/2$
$= 0.69R_{dr}(C_{int}+C_{fan}) + 0.69(R_{dr}c_w+r_wC_{fan})L + 0.38r_wc_wL^2$

- Wire delay rapidly becomes the dominate factor (due to the quadratic term) in the delay budget for longer wires.

Inverter