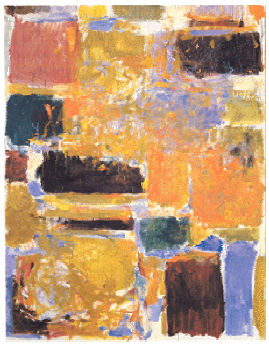


Digital Integrated Circuits

A Design Perspective

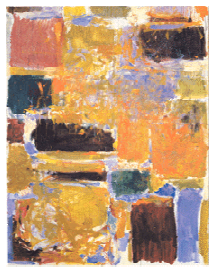
Prentice Hall Electronics and VLSI Series
ISBN 0-13-120764-4

Introduction

[Adapted from Rabaey's *Digital Integrated Circuits*, Second Edition, ©2003 J. Rabaey, A. Chandrakasan, B. Nikolic]

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

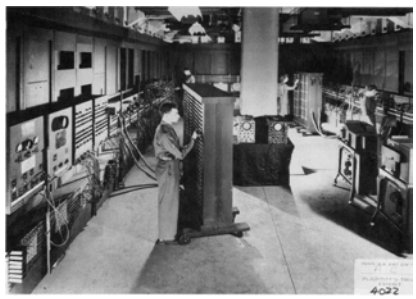


The First Computer

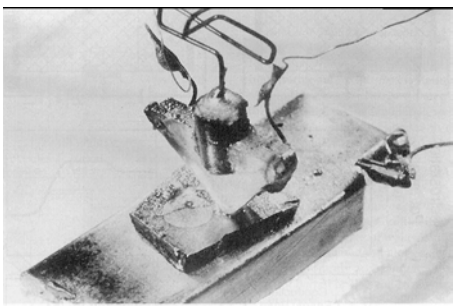
The Babbage Difference Engine (1832)

25,000 parts
cost: £17,470

ENIAC - The First Electronic Computer (1946)

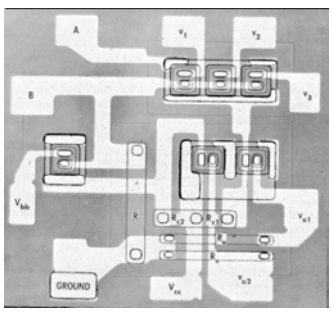


La Révolution du Transistor



Premier transistor
Bell Labs, 1948

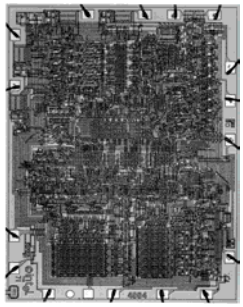
The First Integrated Circuits



Logique Bipolaire des Années 60

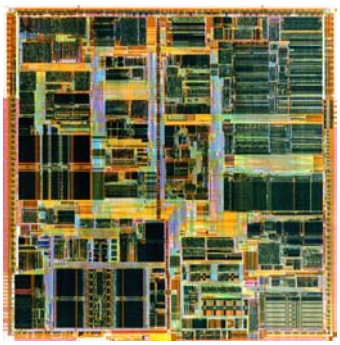
ECL Porte 3-entrées
Motorola 1966

Intel 4004 Micro-processor



1971
2300 transistors
1 MHz operation

Intel Pentium (IV) Microprocessor



Transistor Revolution

- Transistor –Bardeen (Bell labs) in 1947
- Bipolar transistor – Schockley in 1949
- First bipolar digital logic gate – Harris in 1956
- First monolithic IC – Jack Kilby in 1959
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990's
- ECL – 1974 into the 1980's

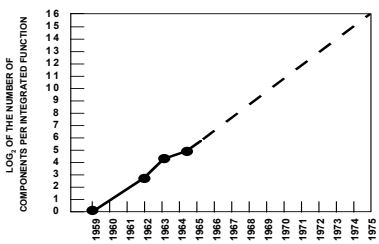
MOSFET Technology

- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, but plagued with manufacturing problems
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – preferred MOSFET technology because of power benefits
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI, Copper-Low K, …

Moore's Law

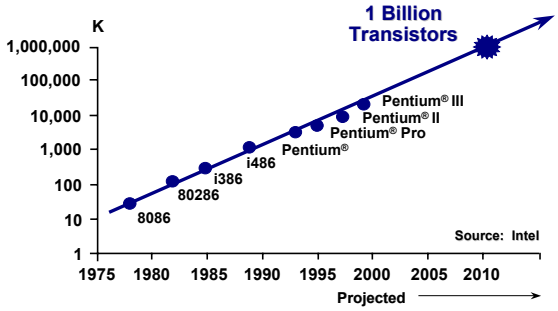
- In 1965, Gordon Moore predicted that the number of transistors that can be integrated on a die would double every 18 to 14 months (i.e., grow exponentially with time).
- Amazingly visionary – million transistor/chip barrier was crossed in the 1980's.
  - 2300 transistors, 1 MHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

Moore's Law



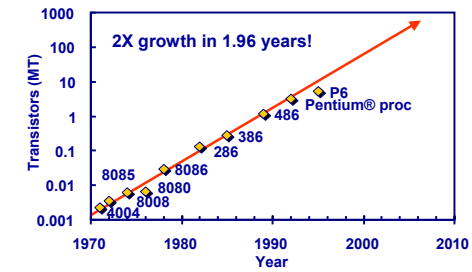
Electronics, April 19, 1965.

Transistor Counts



Courtesy, Intel

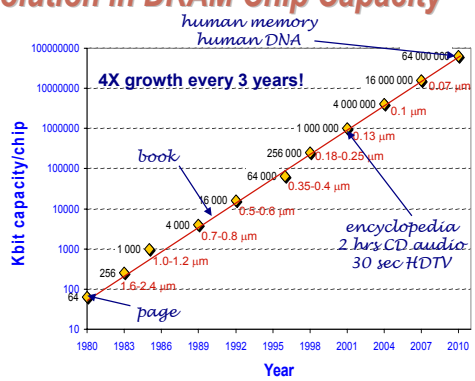
Moore's Law in Microprocessors



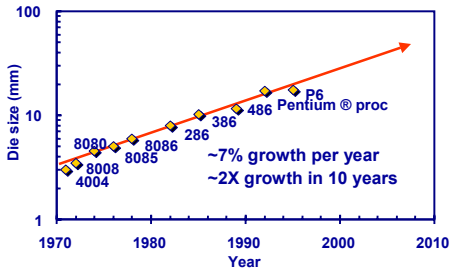
Transistors on Lead Microprocessors double every 2 years

Courtesy, Intel

Evolution in DRAM Chip Capacity



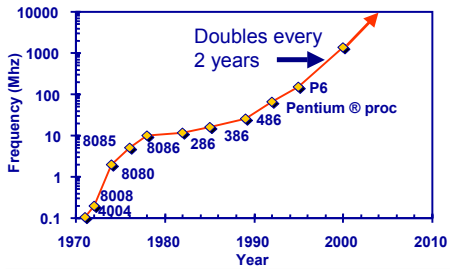
Die Size Growth



Die size grows by 14% to satisfy Moore's Law

Courtesy, Intel

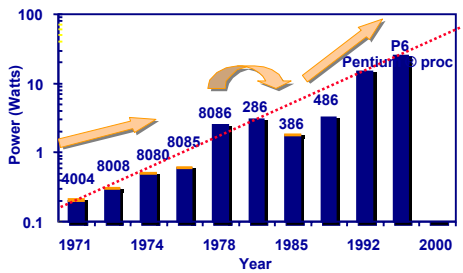
Frequency



Lead Microprocessors frequency doubles every 2 years

Courtesy, Intel

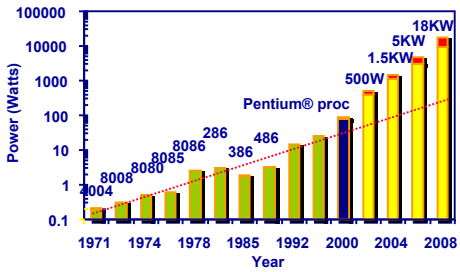
Power Dissipation



Lead Microprocessors power continues to increase

Courtesy, Intel

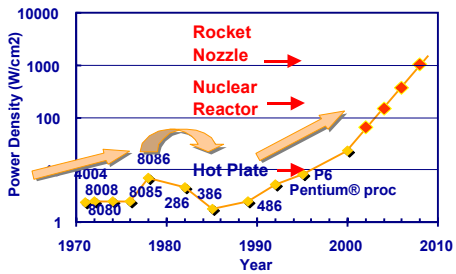
Power Will Be a Major Problem



Power delivery and dissipation will be prohibitive

Courtesy, Intel

Power Density



Power density too high to keep junctions at low temp

Courtesy, Intel

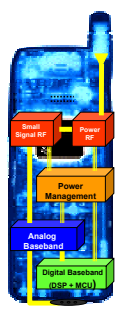
Not Only Microprocessors

Cell Phone

Digital Cellular Market (Phones Shipped)

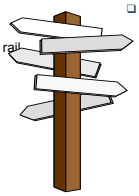
	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Major Design Challenges

- Microscopic issues
  - ultra-high speeds
  - power dissipation and supply rail drop
  - growing importance of interconnect
  - noise, crosstalk
  - reliability, manufacturability
  - clock distribution



- Macroscopic issues
  - time-to-market
  - design complexity (millions of gates)
  - high levels of abstractions
  - design for test
  - reuse and IP, portability
  - systems on a chip (SoC)
  - tool interoperability

Year	Tech.	Complexity	Frequency	3 Yr. Design Staff Size	Staff Costs
1997	0.35	13 M Tr.	400 MHz	210	$90 M
1998	0.25	20 M Tr.	500 MHz	270	$120 M
1999	0.18	32 M Tr.	600 MHz	360	$160 M
2002	0.13	130 M Tr.	800 MHz	800	$360 M

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; Chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Fundamental Design Metrics

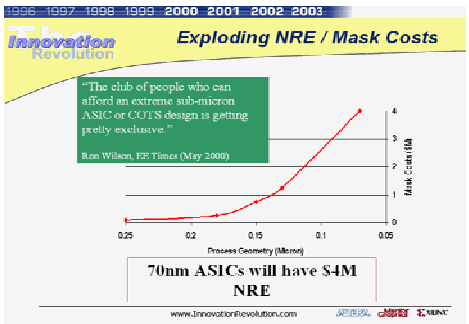
- Functionality
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay)
  - Power consumption; energy
- Time-to-market

Cost of Integrated Circuits

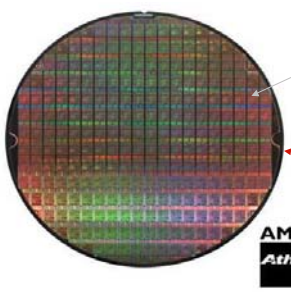
- NRE (non-recurring engineering) costs
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products
- Recurring costs – proportional to product volume
  - silicon processing
    - also proportional to chip area
  - assembly (packaging)
  - test

$$\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}$$

NRE Cost Is Increasing

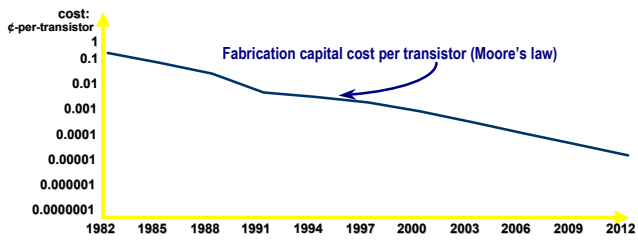


Die Cost



From http://www.amd.com

Cost Per Transistor

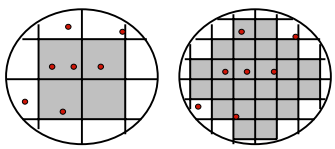


Recurring Costs

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

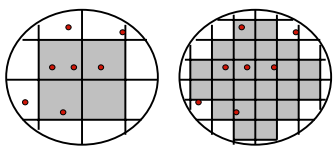
$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}$$

$$\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



$$\text{die yield} = (1 + (\text{defects per unit area} \times \text{die area})/\alpha)^{-\alpha}$$

Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

Yield Example

- Example
  - wafer size of 12 inches, die size of 2.5 cm^2, 1 defects/cm^2, $\alpha = 3$ (measure of manufacturing process complexity)
  - 252 dies/wafer (remember, wafers round & dies square)
  - die yield of 16%
  - 252 x 16% = only 40 dies/wafer die yield !
- Die cost is strong function of die area
  - proportional to the third or fourth power of the die area

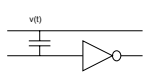
Some Examples (1994)

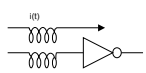
Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Reliability

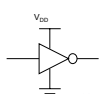
Noise in Digital Integrated Circuits

- Noise – unwanted variations of voltages and currents at the logic nodes
- from two wires placed side by side
  - capacitive coupling
    - voltage change on one wire can influence signal on the neighboring wire
    - cross talk
  - inductive coupling
    - current change on one wire can influence signal on the neighboring wire





- from noise on the power and ground supply rails
  - can influence signal levels in the gate



Example of Capacitive Coupling

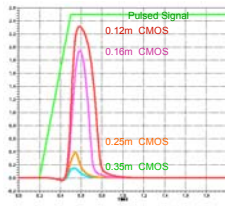
- Signal wire glitches as large as 80% of the supply voltage will be common due to crosstalk between neighboring wires as feature sizes continue to scale

Crosstalk vs. Technology

Black line quiet

Red lines pulsed

Glitches strength vs technology

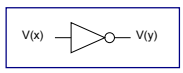


From Dunlop, Lucent, 2000

Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables
  $x \in \{0,1\}$
- A logical variable is associated with a *nominal voltage level* for each logic state

$1 \Leftrightarrow V_{OH}$ and $0 \Leftrightarrow V_{OL}$



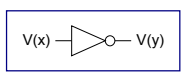
$V_{OH} = !\,(V_{OL})$

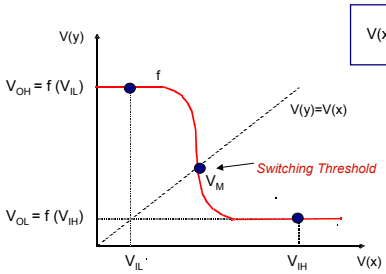
$V_{OL} = !\,(V_{OH})$

- Difference between V_{OH} and V_{OL} is the logic or *signal swing* V_{sw}

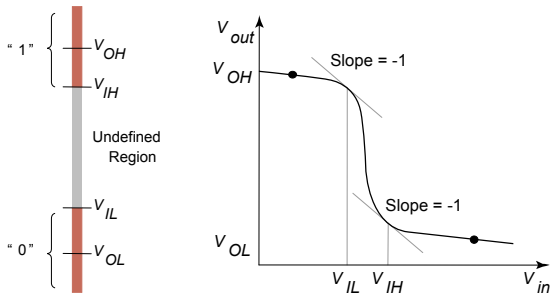
DC Operation
Voltage Transfer Characteristics (VTC)

- Plot of output voltage as a function of the input voltage



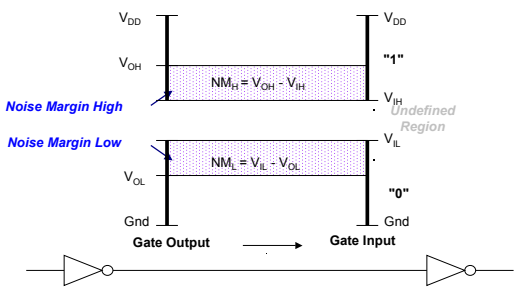


Mapping Between Analog and Digital Signals



Noise Margins

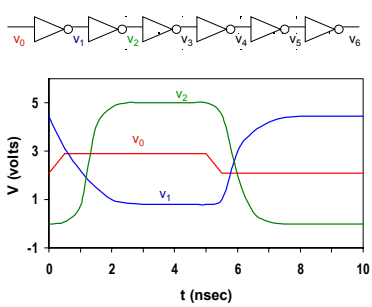
- For robust circuits, want the "0" and "1" intervals to be a s large as possible



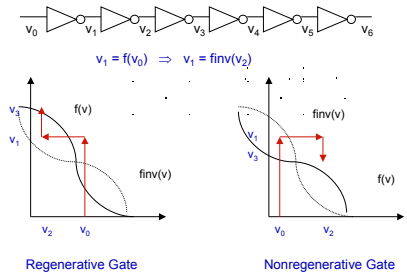
- Large noise margins are desirable, but not sufficient …

The Regenerative Property

- A gate with regenerative property ensure that a disturbed signal converges back to a nominal voltage level



Conditions for Regeneration



Regenerative Gate Nonregenerative Gate

- To be regenerative, the VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.

Noise Immunity

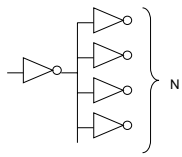
- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, cross talk, interference, offset
- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between V_{OH} and V_{OL}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

Directivity

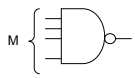
- A gate must be *undirectional*: changes in an output level should not appear at any unchanging input of the same circuit
  - In real circuits *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)
- Key metrics: *output impedance* of the driver and *input impedance* of the receiver
  - ideally, the output impedance of the driver should be zero
  - input impedance of the receiver should be infinity

Fan-In and Fan-Out

- Fan-out – number of load gates connected to the output of the driving gate
  - gates with large fan-out are slower

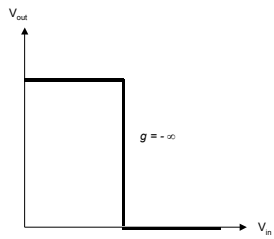


- Fan-in – the number of inputs to the gate
  - gates with large fan-in are bigger and slower



The Ideal Inverter

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.



$R_i = \infty$

$R_o = 0$

Fanout = ∞

$NM_H = NM_L = VDD/2$

An Old-time Inverter

V_{OL}=0.45V

V_{OH}=3.5V

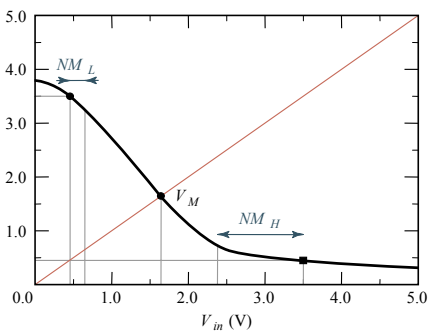
V_{IL}=0.66V

V_{IH}=2.35V

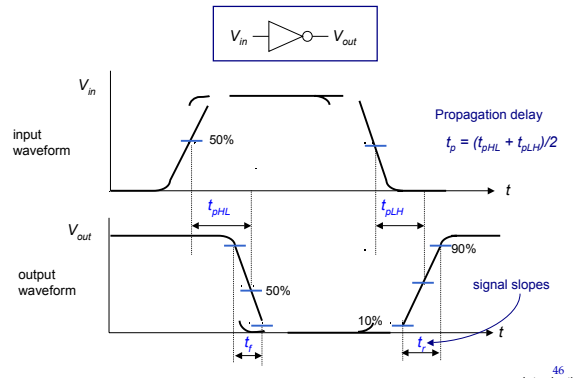
V_M=1.64V

N_{MH}=

N_{ML}=

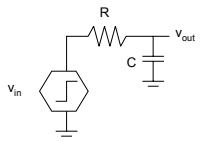


Delay Definitions



Modeling Propagation Delay

- Model circuit as first-order RC network



$v_{out}(t) = (1 - e^{-t/\tau})V$

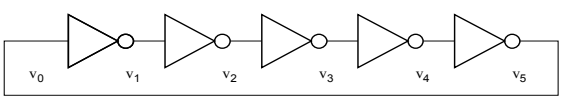
where $\tau = RC$

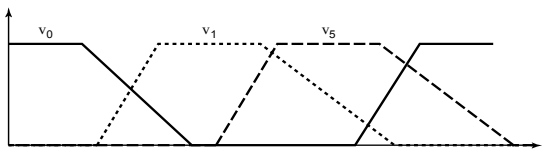
Time to reach 50% point is
$t = \ln(2)\ \tau = 0.69\ \tau$

Time to reach 90% point is
$t = \ln(9)\ \tau = 2.2\ \tau$

- Matches the delay of an inverter gate

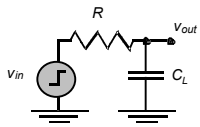
Ring Oscillator : Delay Measurement





$$T = 2 \times t_p \times N$$

A First-order RC Network



$$E_{in} = \int_0^\infty i_{in}(t)v_{in}(t)dt = V\int_0^\infty C_L\frac{dv_{out}}{dt}dt = C_L V\int_0^V dv_{out} = C_L V^2$$

$$E_{C_L} = \int_0^\infty i_{C_L}(t)v_{out}(t)dt = \int_0^\infty C_L\frac{dv_{out}}{dt}v_{out}dt = C_L\int_0^V v_{out}dv_{out} = \frac{C_L V^2}{2}$$

Power and Energy Dissipation

- Power consumption: how much energy is consumed per operation and how much heat the circuit dissipates
  - supply line sizing (determined by peak power)
    $P_{peak} = V_{dd} i_{peak}$
  - battery lifetime (determined by average power dissipation)
    $p(t) = v(t)i(t) = V_{dd} i(t)$ $\quad P_{avg} = 1/T \int p(t)\,dt = V_{dd}/T \int i_{dd}(t)\,dt$
  - packaging and cooling requirements
- Two important components: static and dynamic

$$E\ (\text{joules}) = C_L V_{dd}^2 P_{0\to1} + t_{sc} V_{dd} I_{peak} P_{0\to1} + V_{dd} I_{leakage}$$

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P\ (\text{watts}) = C_L V_{dd}^2 f_{0\to1} + t_{sc} V_{dd} I_{peak} f_{0\to1} + V_{dd} I_{leakage}$$

Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate
- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
  - Power-delay product (PDP) – energy consumed by the gate per switching event
- An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is
  - Energy-delay product (EDP) = power-delay ^{2}

Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation