# Lecture 12

## Circuits numériques (II)

### Circuits inverseurs MOS

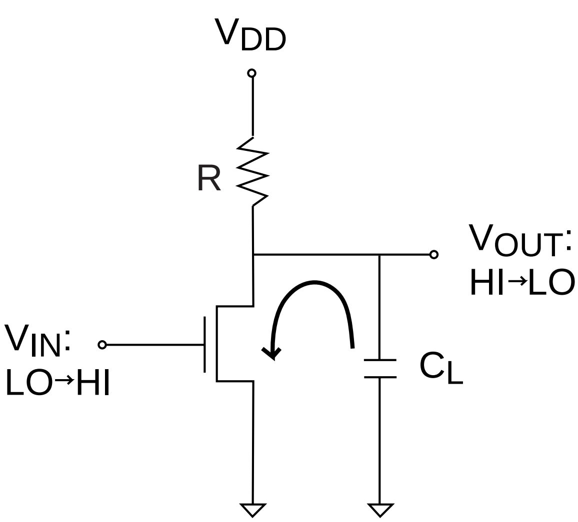
## Outline

- NMOS inverter with resistor pull-up
  - –The inverter
- NMOS inverter with current-source pull-up
- Complementary MOS (CMOS) inverter
- Static analysis of CMOS inverter

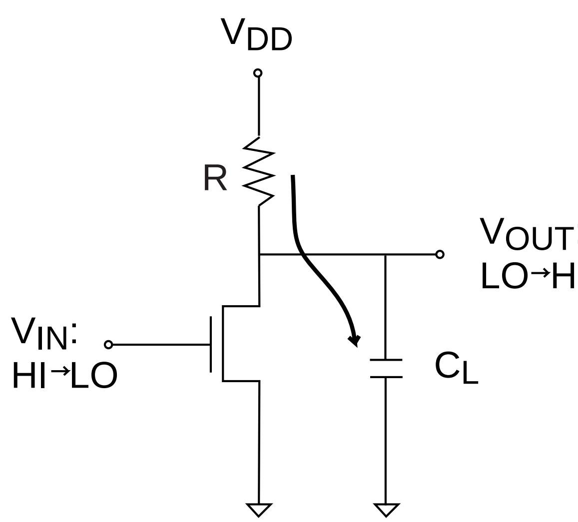
# 1. NMOS inverter with resistor pull-up:

## Dynamics

- $C_L$ ***pull-down*** limited by current through transistor
  - [shall study this issue in detail with CMOS]
- $C_L$ ***pull-up*** limited by resistor ($t_{PLH} \approx RC_L$)
- Pull-up slowest




pull-down




pull-up

# 1. NMOS inverter with resistor pull-up:

## Inverter design issues

Noise margins $\uparrow \Rightarrow |A_v| \uparrow \Rightarrow$

- $R \uparrow \Rightarrow |RC_L| \uparrow \Rightarrow$ slow switching
- $g_m \uparrow \Rightarrow |W| \uparrow \Rightarrow$ big transistor
  - (slow switching at input)

**Trade-off between speed and noise margin.**

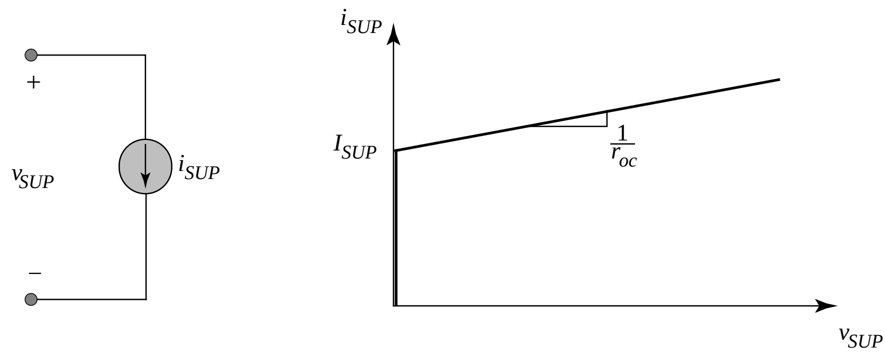
During pull-up we need:

- High current for fast switching
- But also high incremental resistance for high noise margin.

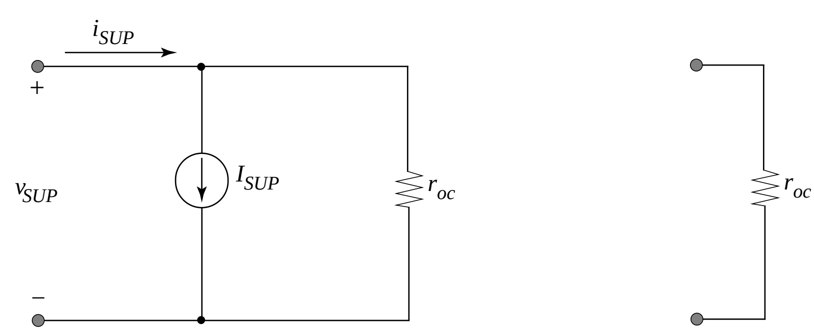
$\Rightarrow$ use ***current source*** as pull-up

# 2. NMOS inverter with current-source pull-up

I—V characteristics of current source:




Equivalent circuit models :



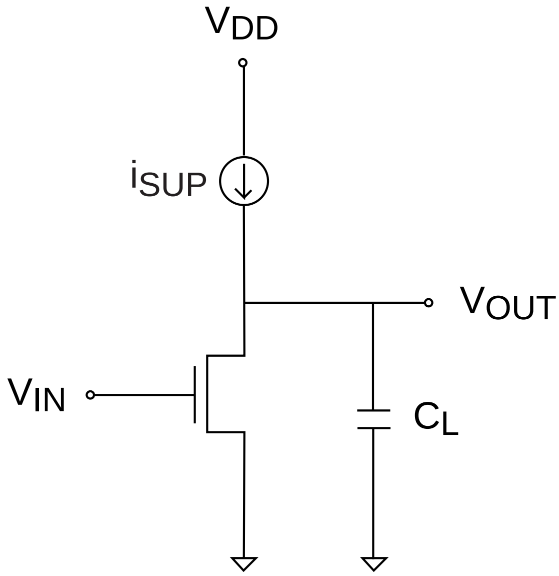

large-signal model

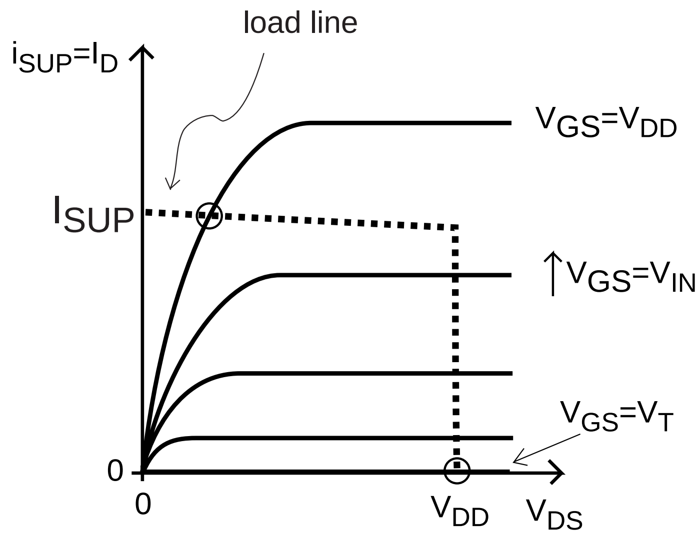
small-signal model

- High current throughout voltage range $v_{SUP} > 0$
- $i_{SUP} = 0$ for $v_{SUP} \leq 0$
- $i_{SUP} = I_{SUP} + v_{SUP}/ r_{oc}$ for $v_{SUP} > 0$
- High small-signal resistance $r_{oc.}$

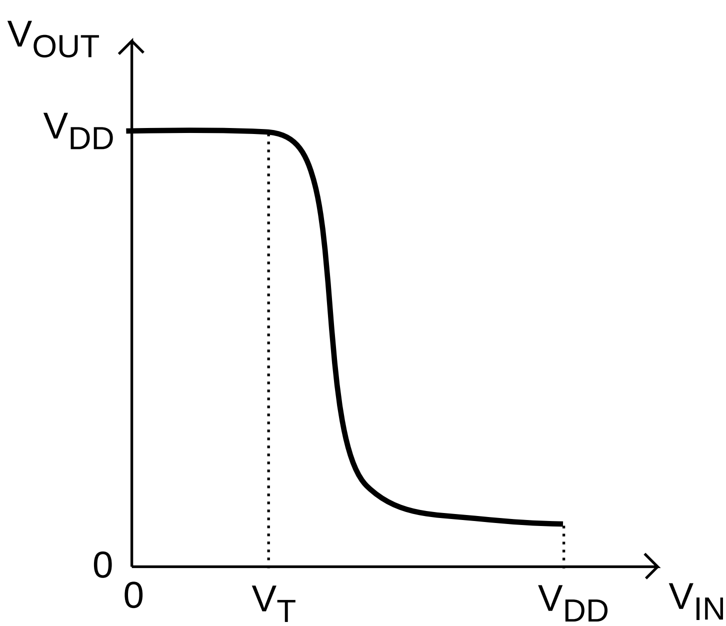
# NMOS inverter with current-source pull-up

## Static Characteristics



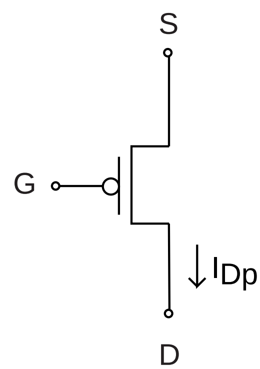

## Inverter characteristics :

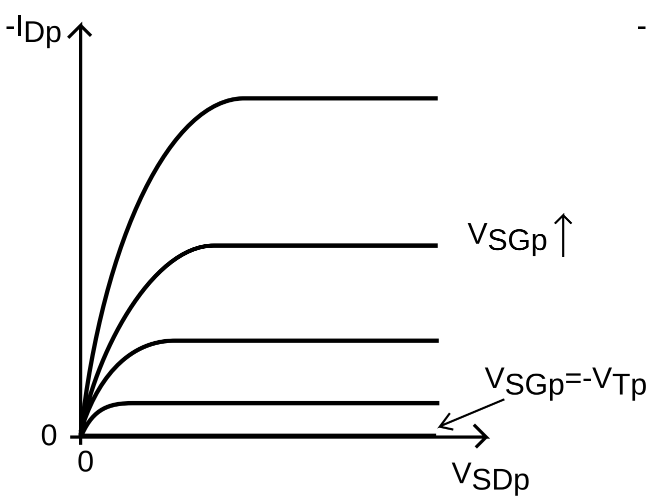


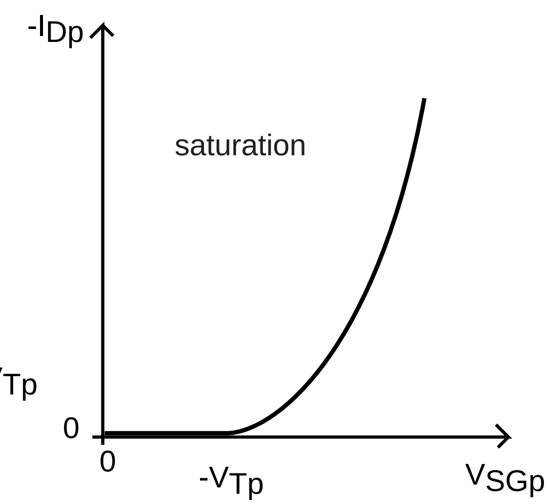

High $r_{oc} \Rightarrow$ high noise margins

# PMOS as current-source pull-up

I—V characteristics of PMOS:



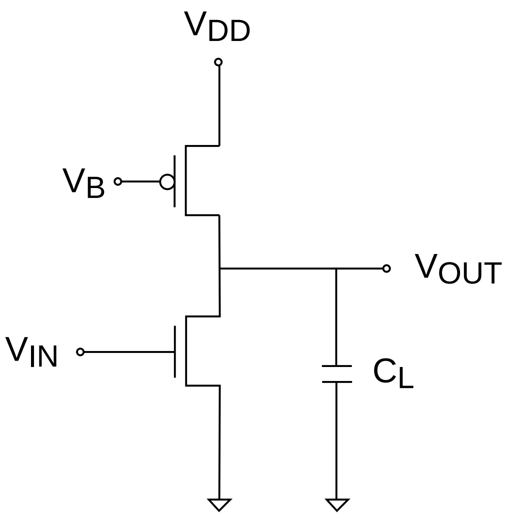

Note: enhancement-mode PMOS has $V_{Tp}$ <0.

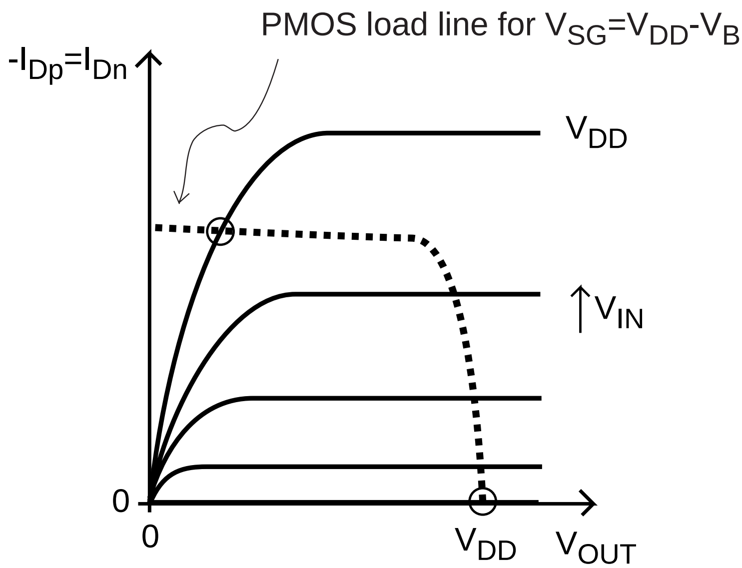
In saturation:

$$-\mathbf{I_{Dp}} \propto \left(\mathbf{V_{SG}} + \mathbf{V_{Tp}}\right)^2$$

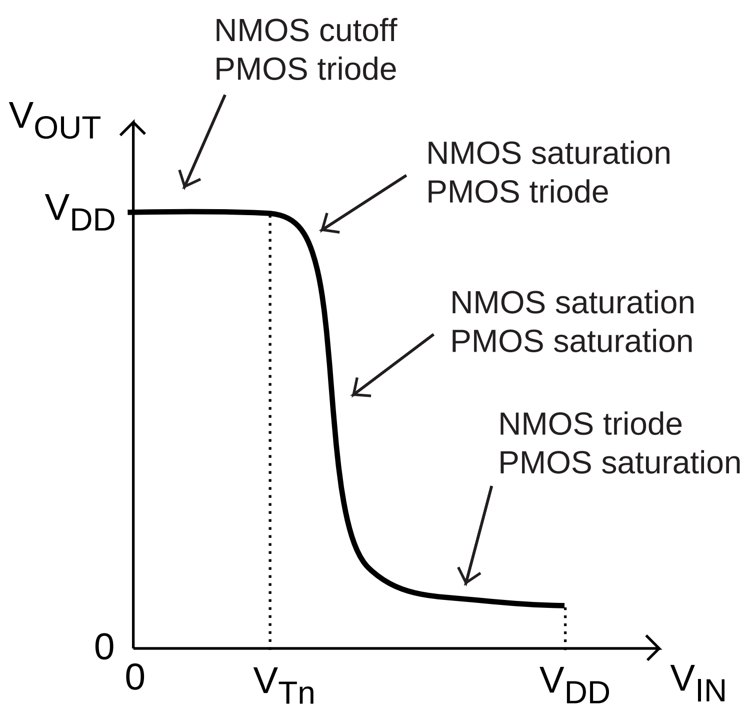
# PMOS as current-source pull-up:

Circuit and load-line diagram of inverter with PMOS current source pull-up:




## Inverter characteristics:



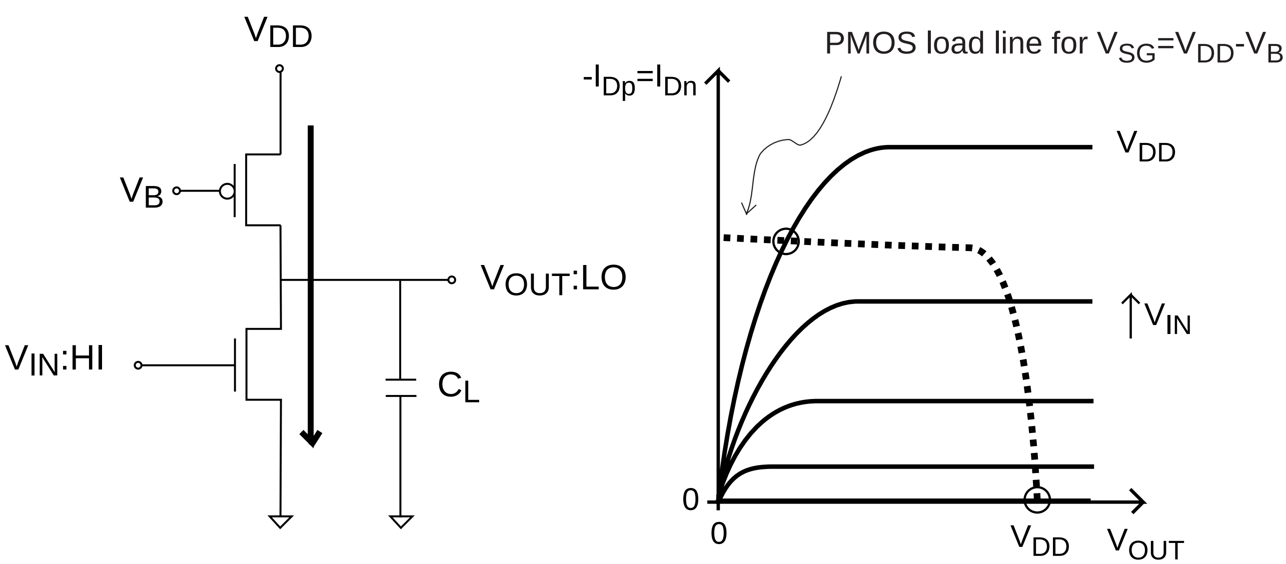
# PMOS as current-source pull-up:

NMOS inverter with current-source pull-up allows high ***noise margin*** with ***fast switching***

- High Incremental resistance
- Constant charging current of load capacitance

But…

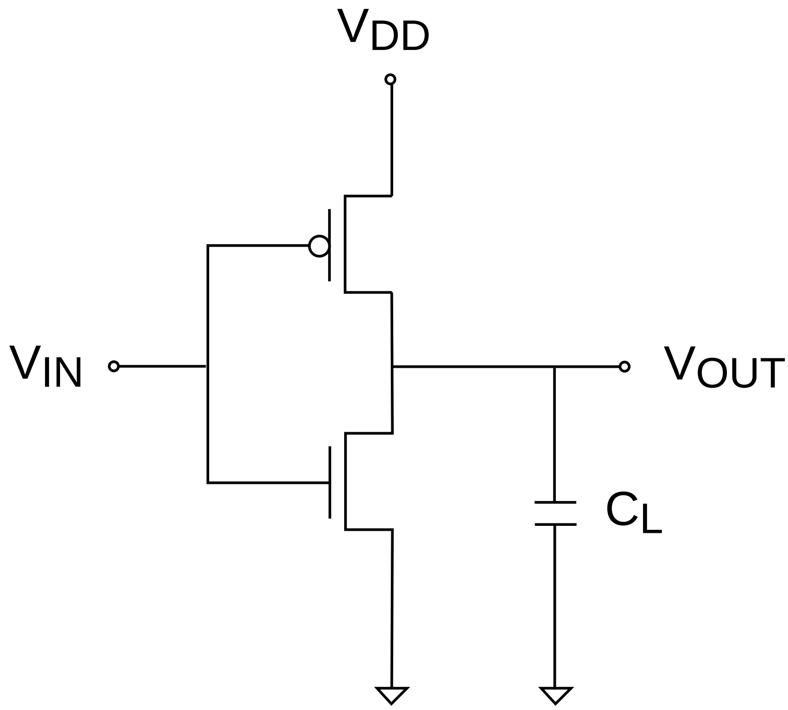
When $V_{IN} = V_{DD}$, there is a direct current path between supply and ground
$\Rightarrow$ power is consumed even if the inverter is idle.




Ideally, we would like to have a current source that is ***itself*** switchable, i.e it shuts off when input is high
$\Rightarrow$ ***CMOS!***

# 3. Complementary MOS (CMOS) Inverter

## Circuit schematic:




Basic Operation:

- $V_{IN} = 0 \quad \Rightarrow \quad V_{OUT} = V_{DD}$

  $V_{GSn} = 0 < V_{Tn} \quad \Rightarrow$ **NMOS OFF**

  $V_{SGp} = V_{DD} > - V_{Tp} \Rightarrow$ **PMOS ON**

- $V_{IN} = V_{DD} \quad \Rightarrow \quad V_{OUT} = 0$

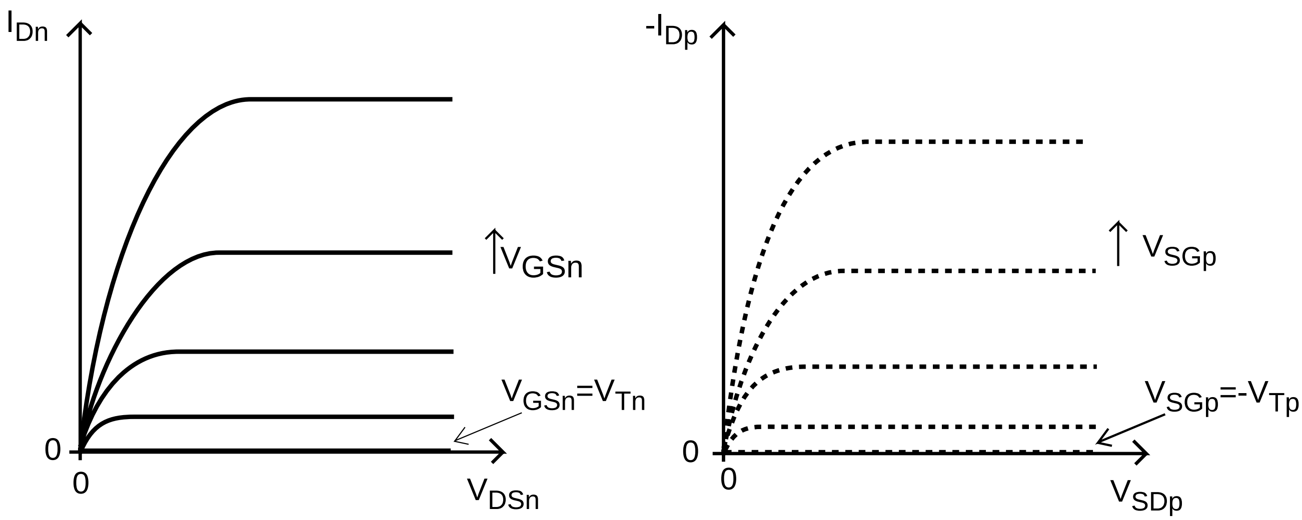
  $V_{GSn} = V_{DD} > V_{Tn} \quad \Rightarrow$ **NMOS ON**

  $V_{SGp} = 0 < - V_{Tp} \quad \Rightarrow$ **PMOS OFF**

**No power consumption while idle in any logic state!**

# CMOS Inverter (Contd.):

Output characteristics of both transistors:




Note:

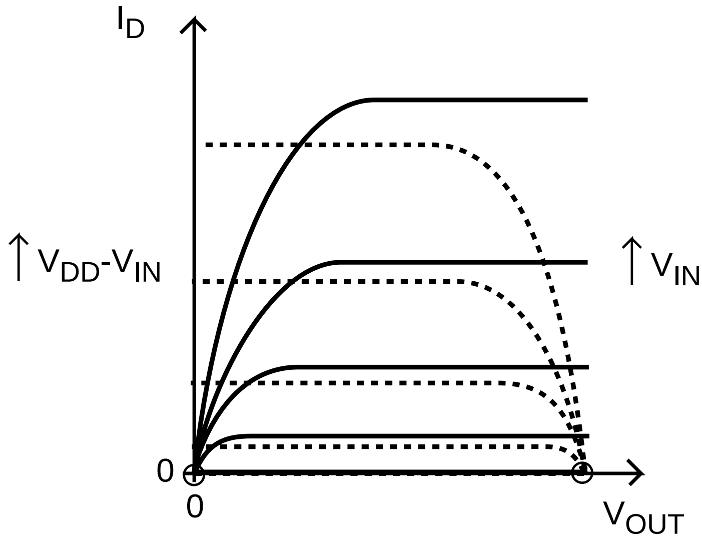
$V_{IN} = V_{GSn} = V_{DD} - V_{SGp} \Rightarrow V_{SGp} = V_{DD} - V_{IN}$

$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp} \Rightarrow V_{SDp} = V_{DD} - V_{OUT}$

$I_{Dn} = -I_{Dp}$

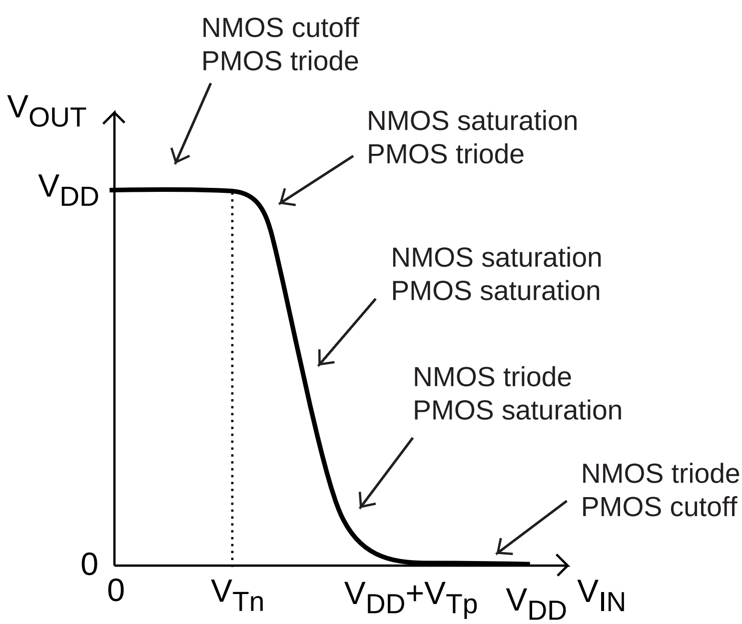
Combine into single diagram of $I_D$ vs. $V_{OUT}$ with $V_{IN}$ as parameter

# CMOS Inverter (Contd.):



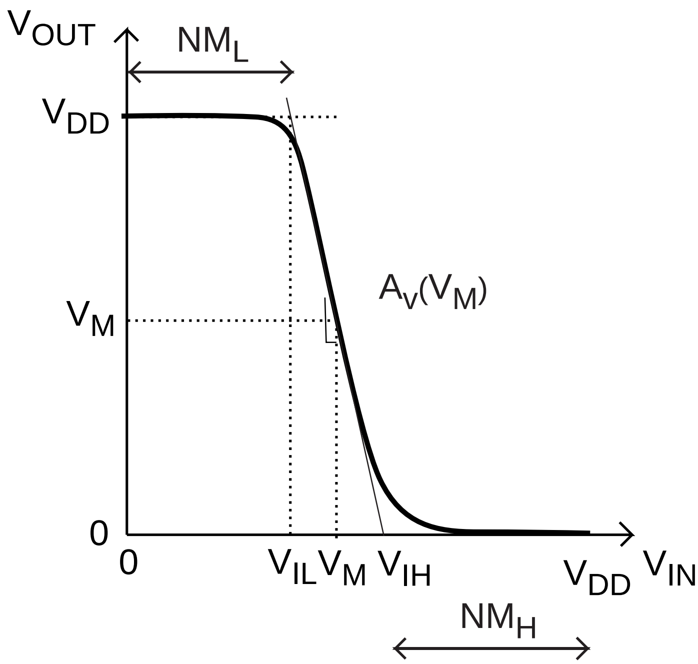

- *No current while idle in any logic state*

## Inverter Characteristics:




- *"rail-to-rail" logic: logic levels are 0 and $V_{DD}$*
- *High $|A_v|$ around logic threshold*
  *$\Rightarrow$ good noise margins*

# 2. CMOS inverter: noise margins




- Calculate $V_M$
- Calculate $A_v(V_M)$
- Calculate $NM_L$ and $NM_H$

## Calculate $V_M$ ($V_M = V_{IN} = V_{OUT}$)

At $V_M$ both transistors are saturated:

$$\mathbf{I_{Dn}} = \frac{\mathbf{W_n}}{2\mathbf{L_n}}\mu_\mathbf{n}\mathbf{C_{ox}}\left(\mathbf{V_M} - \mathbf{V_{Tn}}\right)^2$$

$$-\mathbf{I_{Dp}} = \frac{\mathbf{W_p}}{2\mathbf{L_p}}\mu_\mathbf{p}\mathbf{C_{ox}}\left(\mathbf{V_{DD}} - \mathbf{V_M} + \mathbf{V_{Tp}}\right)^2$$

# CMOS inverter: noise margins (contd.)

Define:

$$\mathbf{k_n} = \frac{\mathbf{W_n}}{\mathbf{L_n}} \mu_n \mathbf{C_{ox}}; \qquad \mathbf{k_p} = \frac{\mathbf{W_p}}{\mathbf{L_p}} \mu_p \mathbf{C_{ox}}$$

Since :

$$\mathbf{I_{Dn}} = -\mathbf{I_{Dp}}$$

Then:

$$\frac{1}{2}\mathbf{k_n}\left(\mathbf{V_M} - \mathbf{V_{Tn}}\right)^2 = \frac{1}{2}\mathbf{k_p}\left(\mathbf{V_{DD}} - \mathbf{V_M} + \mathbf{V_{Tp}}\right)^2$$

Solve for $V_M$:

$$\mathbf{V_M} = \frac{\mathbf{V_{Tn}} + \sqrt{\frac{\mathbf{k_p}}{\mathbf{k_n}}}\left(\mathbf{V_{DD}} + \mathbf{V_{Tp}}\right)}{1 + \sqrt{\frac{\mathbf{k_p}}{\mathbf{k_n}}}}$$

Usually, $V_{Tn}$ and $V_{Tp}$ fixed and $V_{Tn}$ = - $V_{Tp}$
$\Rightarrow$ $V_M$ engineered through $k_p/k_n$ ratio.

# CMOS inverter: noise margins (contd..)

- **Symmetric case**: $k_n = k_p$

$$\mathbf{V_M} = \frac{\mathbf{V_{DD}}}{2}$$

This implies (2<k<3):

$$\frac{\mathbf{k_p}}{\mathbf{k_n}} = 1 = \frac{\frac{\mathbf{W_p}}{\mathbf{L_p}}\mu_{\mathbf{p}}\mathbf{C_{ox}}}{\frac{\mathbf{W_n}}{\mathbf{L_n}}\mu_{\mathbf{n}}\mathbf{C_{ox}}} \approx \frac{\frac{\mathbf{W_p}}{\mathbf{L_p}}\mu_{\mathbf{p}}}{\frac{\mathbf{W_n}}{\mathbf{L_n}}k.\mu_{\mathbf{p}}} \Rightarrow \frac{\mathbf{W_p}}{\mathbf{L_p}} \approx k\frac{\mathbf{W_n}}{\mathbf{L_n}}$$

Since usually $L_p \approx L_n = L_{min} \Rightarrow W_p \approx k.W_n$

- **Asymmetric case**: $\mathbf{k_n >> k_p}$, **or** $\frac{\mathbf{W_n}}{\mathbf{L_n}} >> \frac{\mathbf{W_p}}{\mathbf{L_p}}$

$$\mathbf{V_M \approx V_{Tn}}$$

NMOS turns on as soon as $V_{IN}$ goes above $V_{Tn}$.

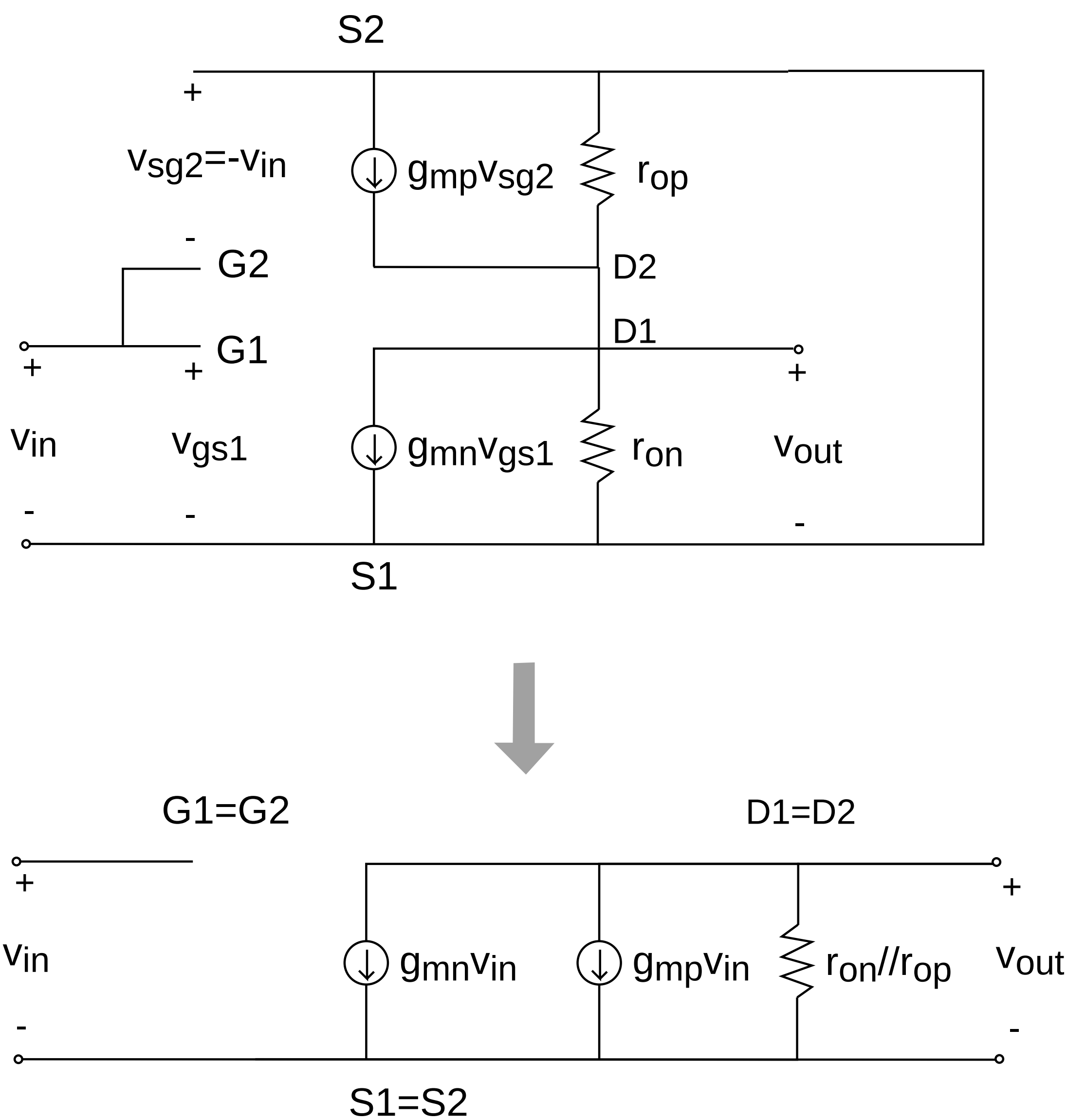
- **Asymmetric case**: $\mathbf{k_n << k_p}$, **or** $\frac{\mathbf{W_n}}{\mathbf{L_n}} << \frac{\mathbf{W_p}}{\mathbf{L_p}}$

$$\mathbf{V_M \approx V_{DD} + V_{Tp}}$$

PMOS turns on as soon as $V_{IN}$ goes below $V_{DD} + V_{Tp}$.

# CMOS inverter: noise margins (contd…)
# Calculate $A_v(V_M)$

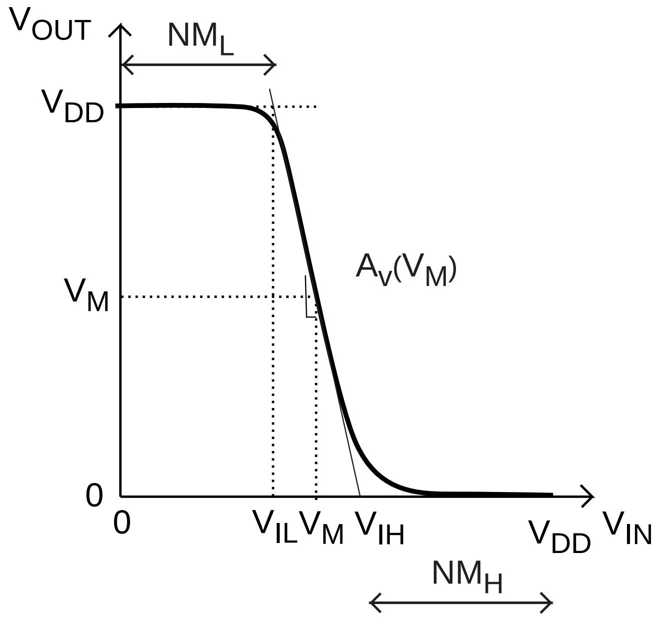
- Small signal model:




$$A_v = -\left(g_{mn} + g_{mp}\right)\left(r_{on} // r_{op}\right)$$

This can be rather large.

# CMOS inverter: calculate noise margins (contd.)




- Noise-margin low, $NM_L$:

$$\mathbf{V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}}$$

$$\mathbf{NM_L = V_{IL} - V_{OL} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}}$$

- Noise-margin high, $NM_H$:

$$\mathbf{V_{IH} = V_M \left(1 + \frac{1}{|A_v|}\right)}$$

$$\mathbf{NM_H = V_{OH} - V_{IH} = V_{DD} - V_M \left(1 + \frac{1}{|A_v|}\right)}$$

# What did we learn today?

## Summary of Key Concepts

- In NMOS inverter with resistor pull-up, there is a trade-off between noise margin and speed
- Trade-off resolved using current source pull-up
  - **Use PMOS as current source**.
- In NMOS inverter with current-source pull-up: if $V_{IN}$ = High, there is power consumption even if inverter is idling.
- Complementary MOS: **NMOS and PMOS switch-on alternatively**.
  - No current path between power supply and ground
  - No power consumption while idling
- Calculation of CMOS
  - $V_M$
  - Noise Margin