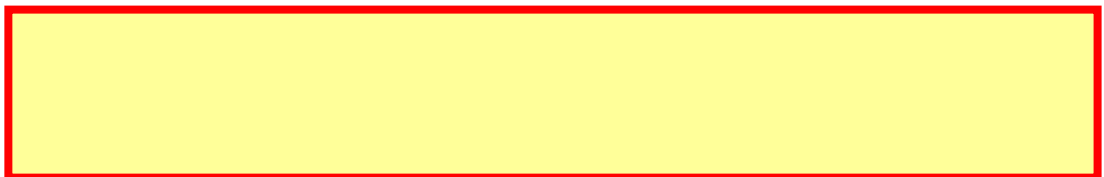# Lecture 11
Circuits numériques (I)
L'inverseur
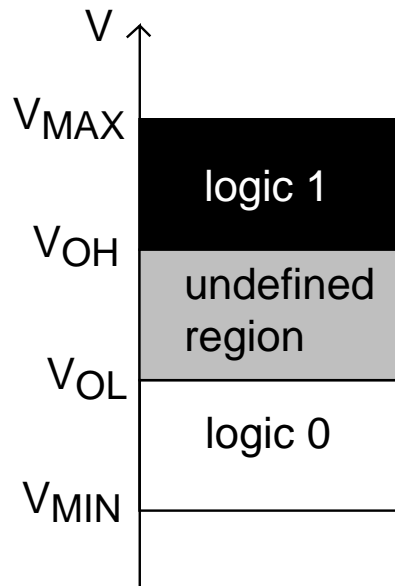
Outline

- Introduction to digital circuits
    - The inverter
- NMOS inverter with resistor pull-up

1. Introduction to digital circuits: the inverter

In digital circuits, digitally-encoded information is represented by means of two distinct voltage ranges:
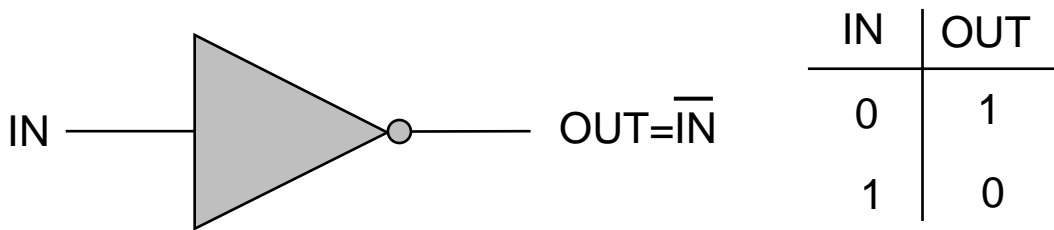

The Static Definition

- *Logic 0:* $V_{MIN} \leq V \leq V_{OL}$

- *Logic 1:* $V_{OH} \leq V \leq V_{MAX}$

- *Undefined logic value:* $V_{OL} \leq V \leq V_{OH}$
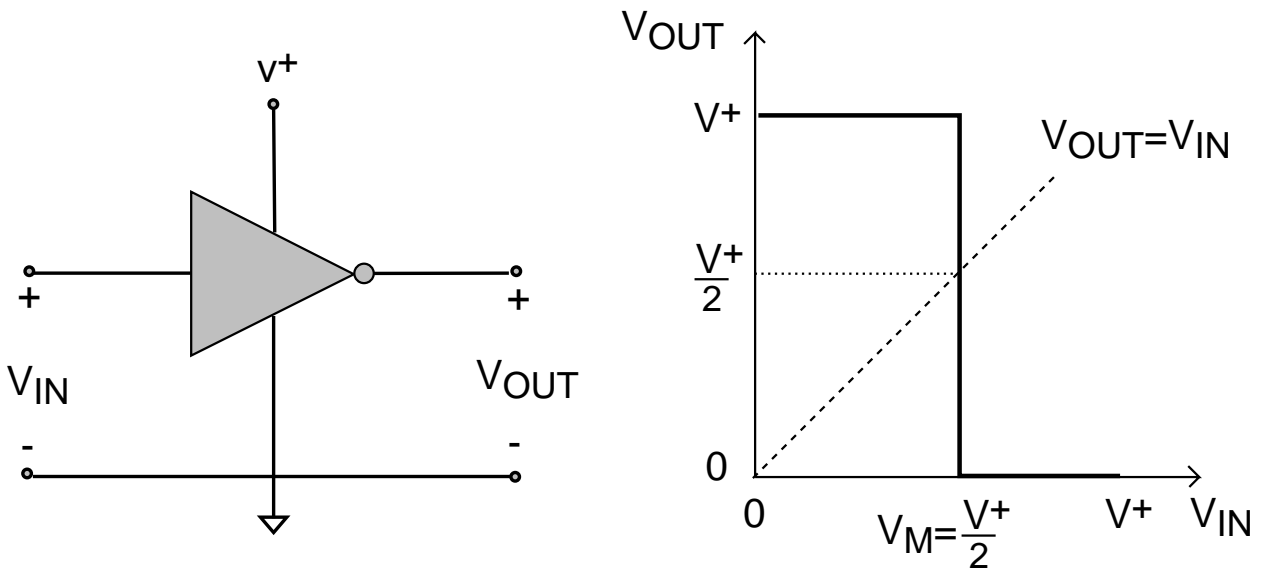
Logic operations are performed using *logic gates*.

Simplest logic operation of all: *inversion* $\Rightarrow$ inverter

Ideal inverter

IN	OUT
0	1
1	0

$$OUT = \overline{IN}$$

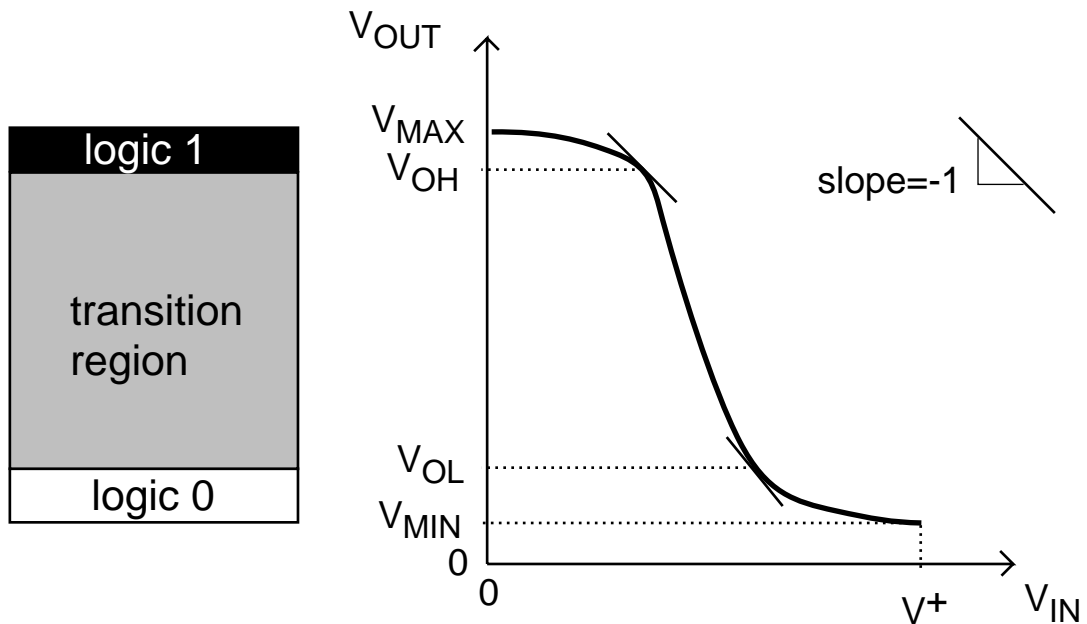Circuit representation and ideal transfer function:

Define *switching point* or *logic threshold* :

- $V_M \equiv$ input voltage for which $V_{OUT} = V_{IN}$
  - For $0 \leq V_{IN} < V_M \quad \Rightarrow V_{OUT} = V^+$
  - For $V_M < V_{IN} \leq V^+ \quad \Rightarrow V_{OUT} = 0$

Ideal inverter returns well defined logical outputs (0 or V^+) even in the presence of considerable noise in V_{IN} (from voltage spikes, crosstalk, etc.)
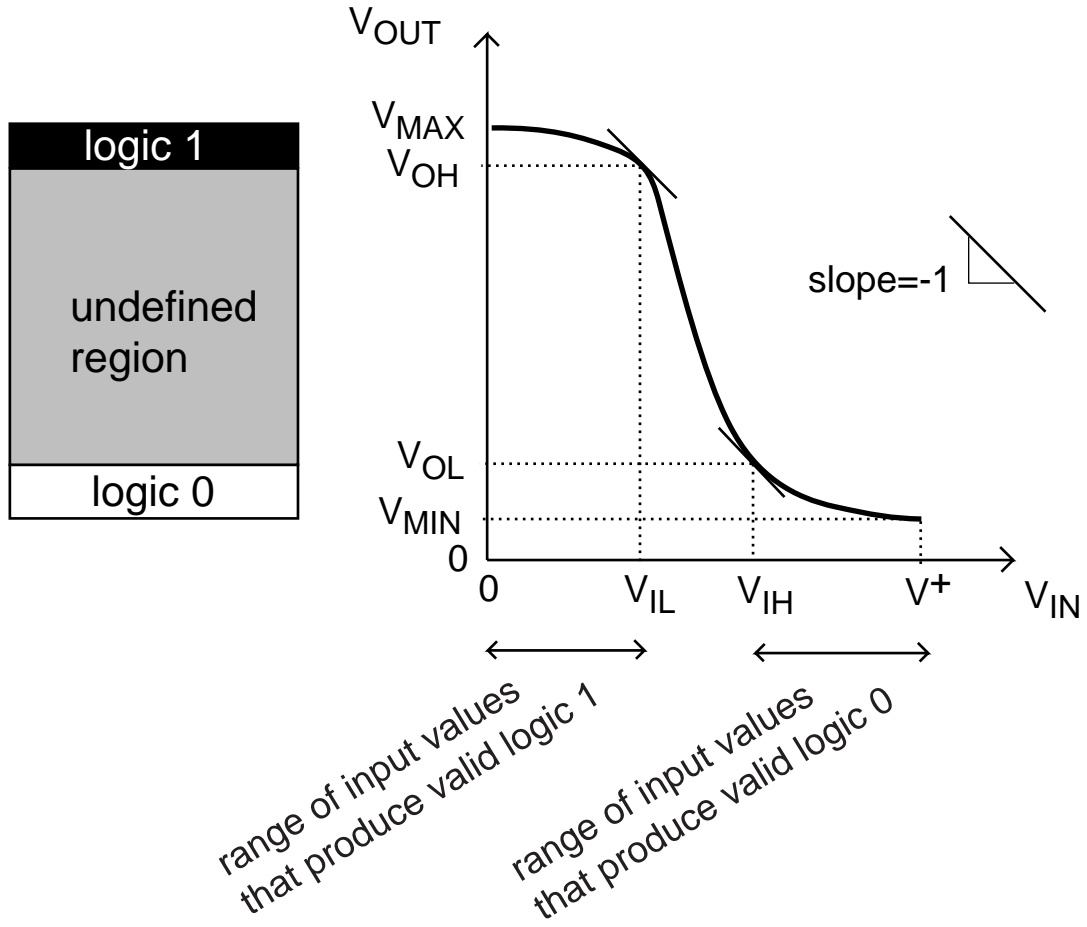$\Rightarrow$ signal is *regenerated*!

"Real" inverter

In a real inverter, valid logic levels defined as follows:

- Logic 0:
    - $V_{MIN} \equiv$ output voltage for which $V_{IN} = V^+$
    - $V_{OL} \equiv$ smallest output voltage where slope = -1
- Logic 1:
    - $V_{OH} \equiv$ largest output voltage where slope = -1
    - $V_{MAX} \equiv$ output voltage for which $V_{IN} = 0$
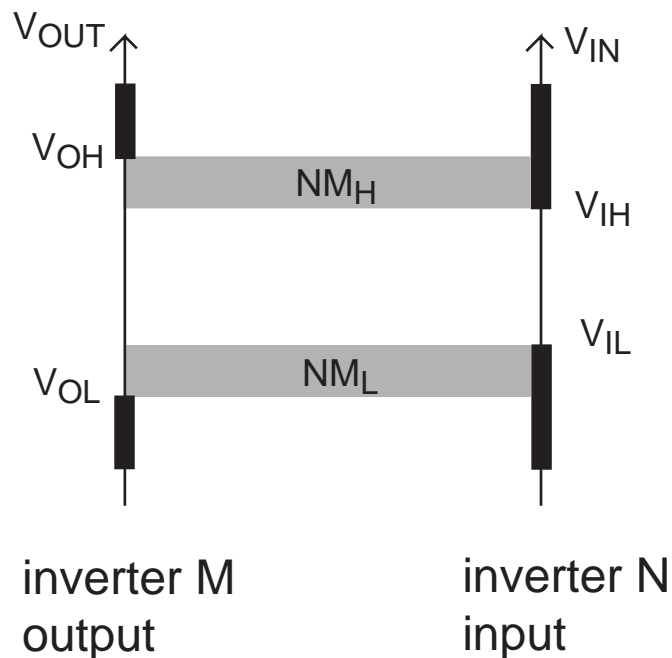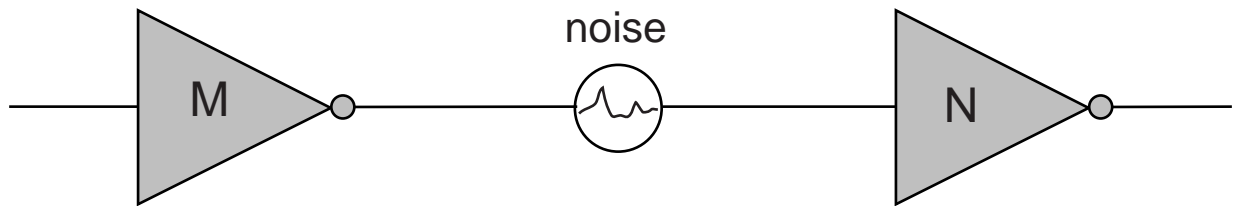
Two other important voltages:

Define:

$V_{IL} \equiv$ smallest input voltage where slope = -1
$V_{IH} \equiv$ highest input voltage where slope = -1

If range of output values V_{OL} to V_{OH} is ***wider*** than the range of input values V_{IL} to V_{IH}, then the inverter exhibits some noise immunity. (|Voltage gain| > 1)

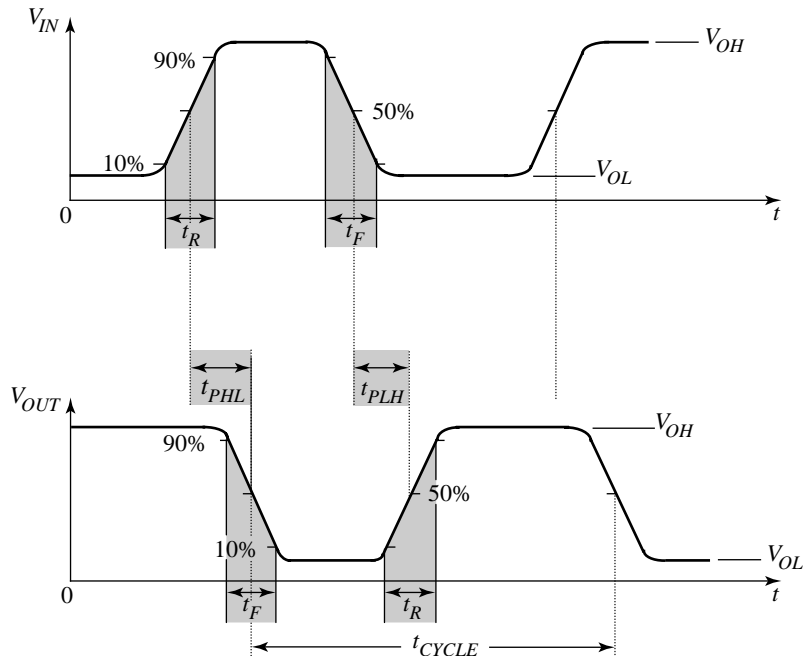Quantify this through ***noise margins***.

Chain of two inverters:

Define *noise margins*:

$$NM_H \equiv V_{OH} - V_{IH}$$ noise margin high
$$NM_L \equiv V_{IL} - V_{OL}$$ noise margin low

Transient Characteristics

Inverter switching in the time domain:

t_R $\equiv$ *rise time* between 10% and 90% of total swing

t_F $\equiv$ *fall time* between 90% and 10% of total swing

t_{PHL} $\equiv$ *propagation delay from high-to-low* between 50% points

t_{PLH} $\equiv$ *propagation delay from low-to-high* between 50% points
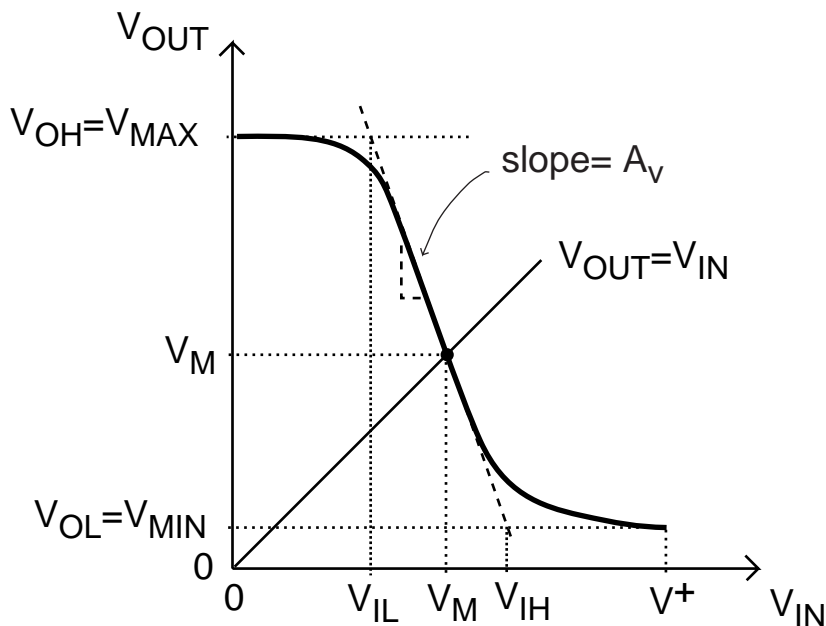
Propagation delay : $\quad \mathbf{t_P = \dfrac{1}{2}\left(t_{PHL} + t_{PLH}\right)}$

Simplifications for hand calculations:
Logic levels and noise margins

It is hard to compute points in transfer function with slope = -1.

Approximate in the following way:

- Assume $V_{OL} \approx V_{MIN}$ and $V_{OH} \approx V_{MAX}$
- Trace tangent of transfer function at V_M
  - Slope = small signal voltage gain (A_v) at V_M
- $V_{IL} \approx$ intersection of tangent with $V_{OUT} = V_{MAX}$
- $V_{IH} \approx$ intersection of tangent with $V_{OUT} = V_{MIN}$
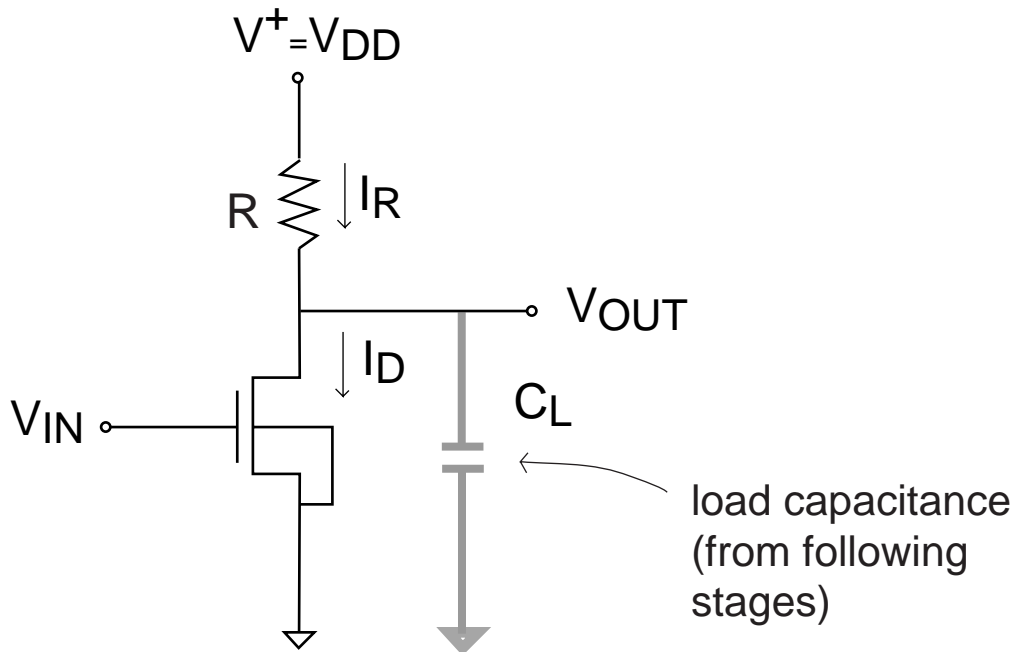
Simplifications for hand calculations:
Propagation delay

- Consider input waveform is an ideal square wave
- Propagation delay times = delay times to 50% point
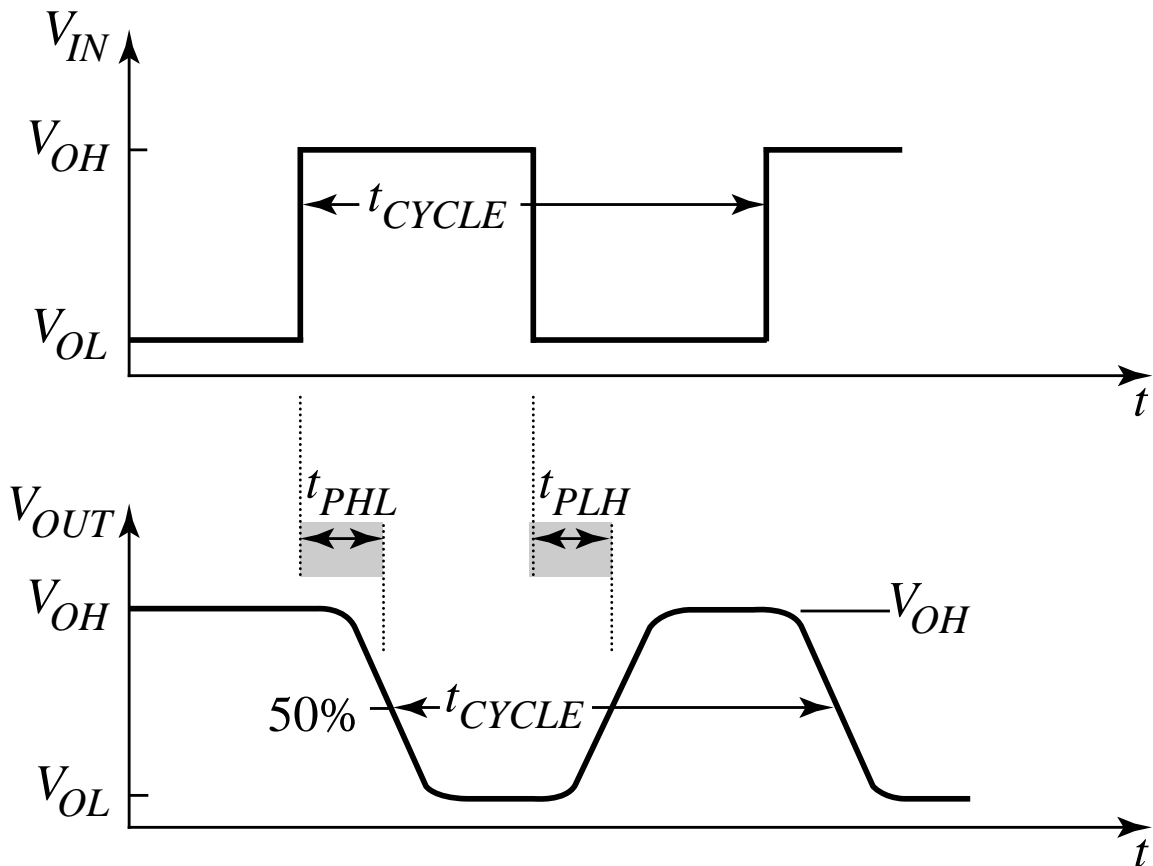
- Hand calculations rather difficult
- SPICE essential for accurate delay analysis
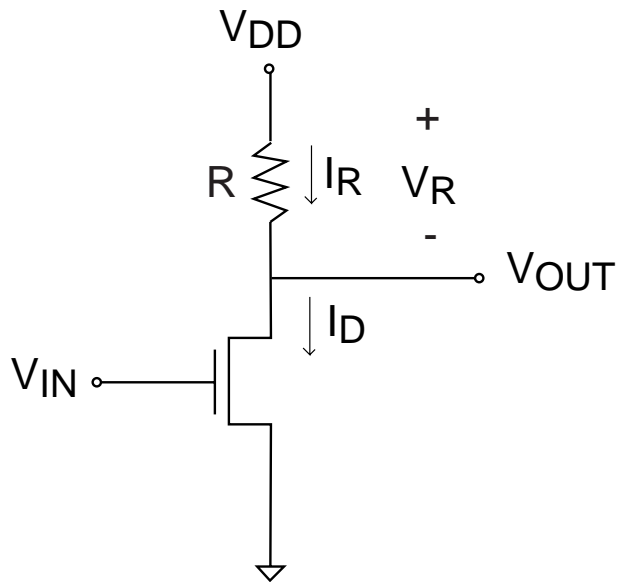
2. NMOS inverter with "pull-up" resistor

Essential features:

- $V_{BS} = 0$ (typically not shown)
- C_L summarizes capacitive loading of the following stages (other logic gates, interconnect lines, etc.)
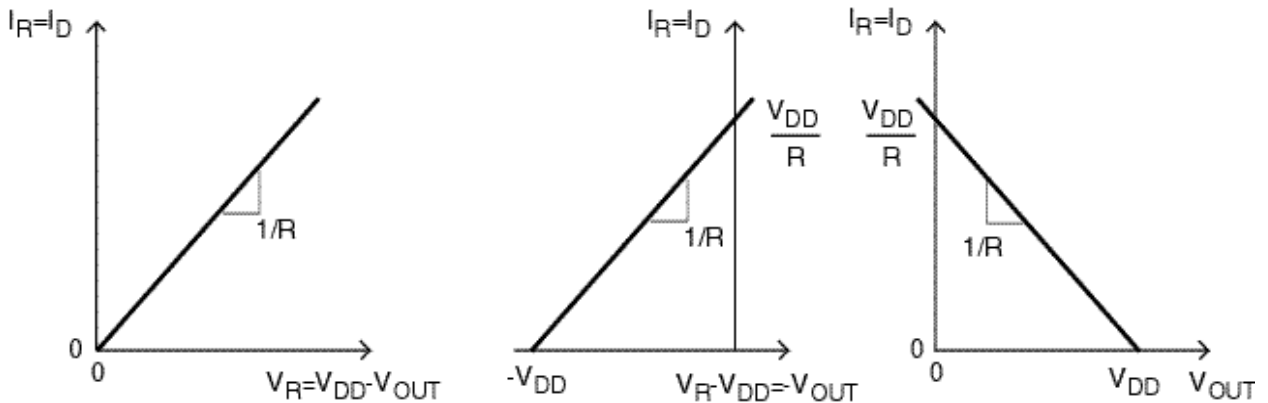
Basic Operation:

- If $V_{IN} < V_T$, MOSFET is **OFF**
  - $\Rightarrow V_{OUT} = V_{DD}$
- If $V_{IN} > V_T$, MOSFET is **ON**
  - $\Rightarrow V_{OUT}$ small
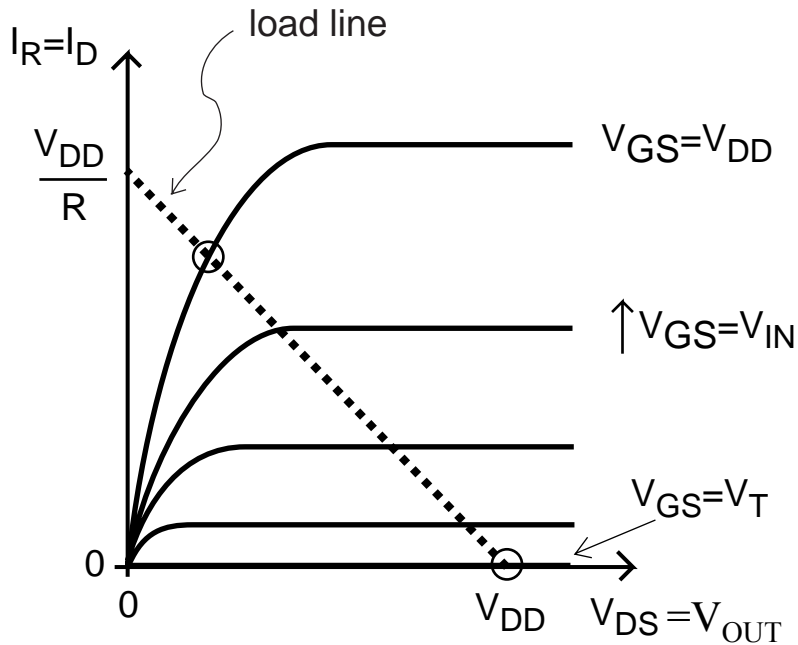 - Value set by resistor / nMOS divider

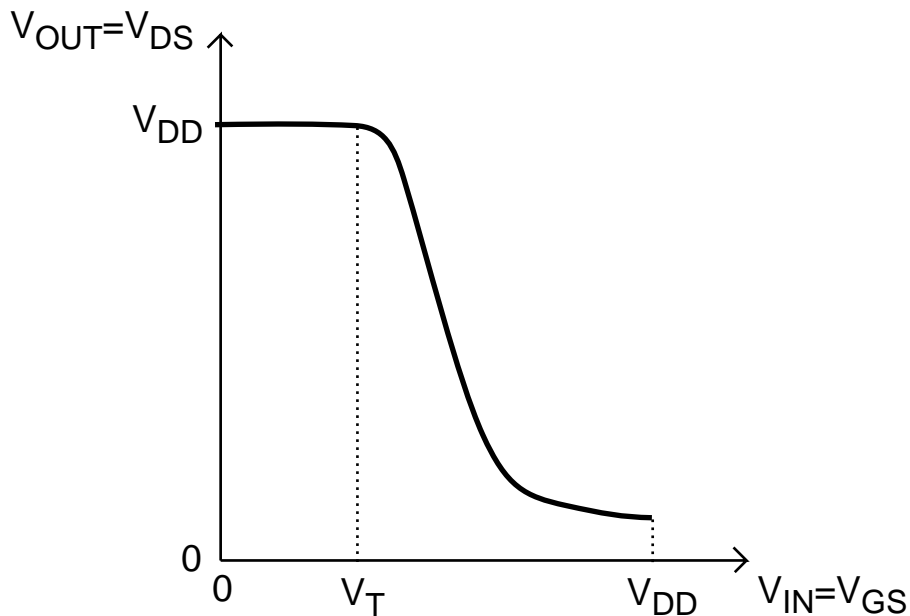Transfer function obtained by solving:

$$I_R = I_D$$

Can solve graphically: I–V characteristics of load:

Overlap I–V characteristics of resistor pull-up on I–V
characteristics of transistor:

load line

$I_R = I_D$

$\dfrac{V_{DD}}{R}$

$V_{GS} = V_{DD}$

$\uparrow V_{GS} = V_{IN}$

$V_{GS} = V_T$

0

0

V_{DD}

$V_{DS} = V_{OUT}$

Transfer function:

$V_{OUT} = V_{DS}$

V_{DD}

0

0   V_T V_{DD} $V_{IN} = V_{GS}$

Logic levels:
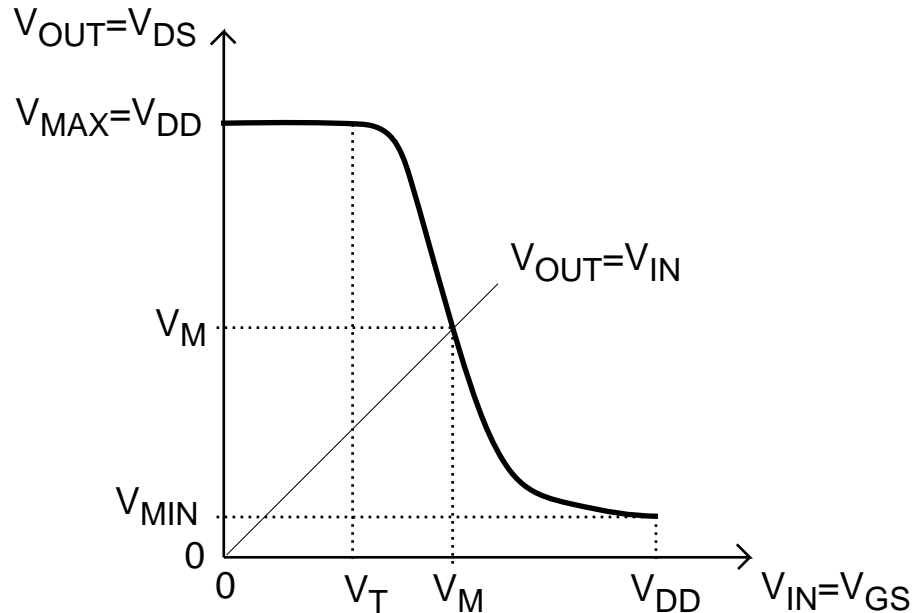
For V_{MAX}, transistor is cut-off, $I_D = 0$:

$$V_{MAX} = V_{DD}$$

For V_{MIN}, transistor is in linear regime; solve:

$$\mathbf{I_D} = \frac{\mathbf{W}}{\mathbf{L}}\, \mu_n \mathbf{C_{ox}}\!\left(\mathbf{V_{DD}} - \frac{\mathbf{V_{MIN}}}{2} - \mathbf{V_T}\right)\!\mathbf{V_{MIN}} = \mathbf{I_R} = \frac{\mathbf{V_{DD}} - \mathbf{V_{MIN}}}{\mathbf{R}}$$

For V_M, transistor is in saturation; solve:

$$\mathbf{I_D} = \frac{\mathbf{W}}{2\mathbf{L}}\, \mu_n \mathbf{C_{ox}}\!\left(\mathbf{V_M} - \mathbf{V_T}\right)^2 = \mathbf{I_R} = \frac{\mathbf{V_{DD}} - \mathbf{V_M}}{\mathbf{R}}$$

Noise Margins:
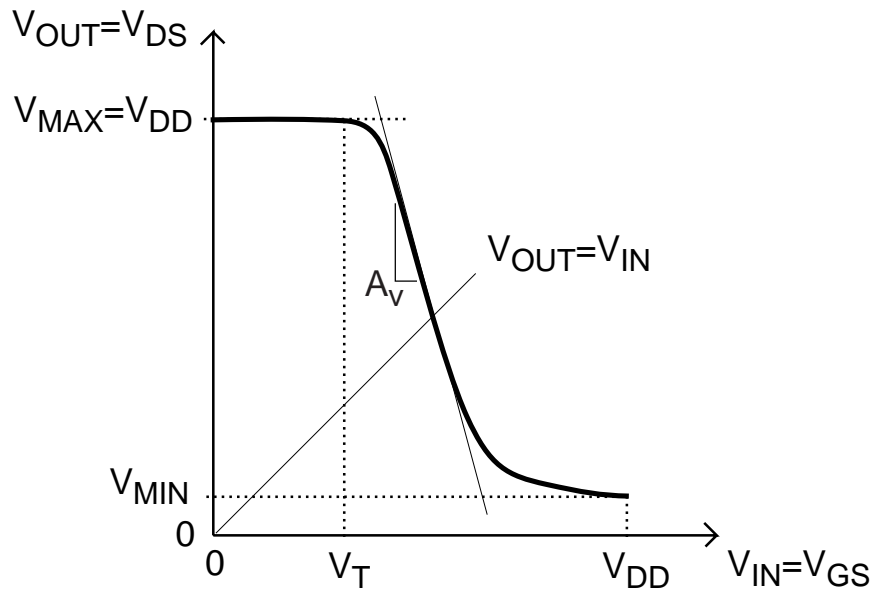
Small signal equivalent circuit model at V_M (transistor in saturation):
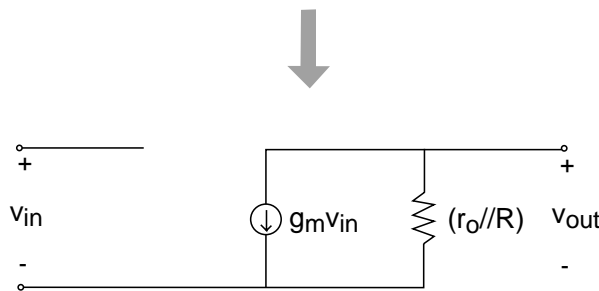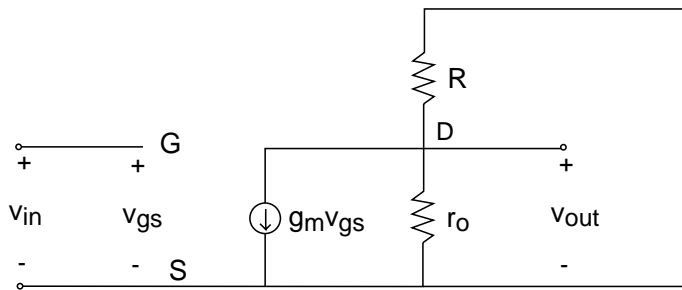
$$A_v = \frac{v_{out}}{v_{in}} = -g_m(r_o // R) \approx -g_m R$$

What did we learn today?

Summary of Key Concepts

- Logic circuits must exhibit immunity to noise in the input signal
  - *Noise margins*

- Logic circuits must be *regenerative*
  - Able to restore clean logic values even if input is noisy.

- *Propagation delay*: time for logic gate to perform its function.

- Concept of *load line*: graphical technique to visualize transfer characteristics of inverter.

- First-order solution (by hand) of inverter figures-of-merit easy if *regimes of operation* of transistor are correctly identified.

- For more accurate solutions, use SPICE (or other CAD tool).